PNX1005

Media processor

Rev. 01.01C — 18 March 2009 — Objective data sheet

1. General description

The PNX1005 is a software programmable media processor, based on the TriMedia TM3282 Very Long Instruction Word (VLIW) architecture and combined with audio and video peripherals.

PNX1005 permits high-definition video compression and decompression (H.264, MPEG4 and MJPEG), video analysis, video improvement and audio acoustic processing. The PNX1005 processes full 1080p/60 Hz video input and output; it can process up to 16 audio channels.

The TriMedia core has an optimized instruction set to handle entropy coding for H.264, motion estimation for H.264, video analysis, video improvement and acoustic processing, while optimizing the memory bandwidth. The core permits both fixed as well as floating point operations and is fully programmable in standard C/C++.

2. Features

2.1 High-performance TM3282 TriMedia VLIW media processor

- Powerful multimedia instructions for entropy coding, motion estimation and others
- Fixed and floating point instructions
- 128 KB data cache and 64 kB instruction cache

2.2 Supporting the latest audio and video codecs

- H.264, MPEG or MJPEG up to 720p/30 frames per second, dual-channel D1/30 frames per second or 8 channel D1/5 frames per second encoding or decoding
- MPEG2 decoding up to 1080i
- MP3, AAC, Dolby AC-3 etc.
- Multi-channel acoustic processing

2.3 Powerful audio and video inputs and outputs

- Video input permits up to 1080p/60p or 8 channel D1 or bit streams up to 24 bit at 157 MHz
- Video output permits up to 1080p/60 or dual-channel D1
- 16 channels I^2S audio input or output

founded by Philips

2.4 Peripherals

- DDR1 or DDR2 JEDEC compliant interface up to 266 MHz (533 Mb/s)
- Dedicated separated on-chip blocks for scaling, advanced de-interlacing, color space conversion, Bayer pattern conversion etc.; data exchange through internal DMA bus
- PCI 2.2 up to 66 MHz
- Up to 16-bit wide NOR and NAND glueless FLASH interface
- USB 2.0 HS OTG
- Programmable GPIO pins for serial protocols like UARTs, SD card or SPI

2.5 Software

- Fully programmable in C/C++
- Easy-to-use development tools with graphical environment integrated into Eclipse
- Complete SDK available from NXP

3. Applications

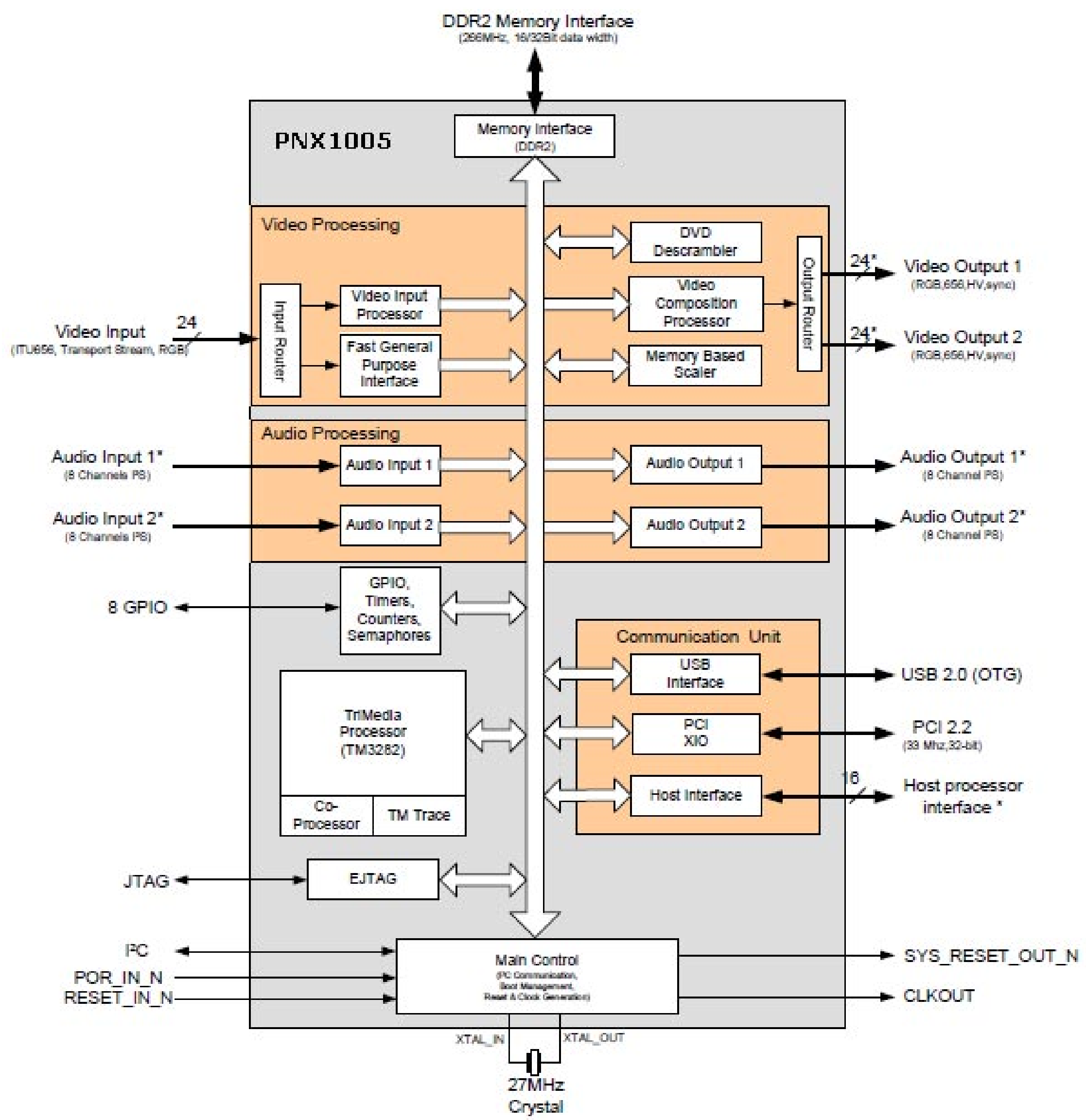
- Security and surveillance (CCTV)
- Audio and video conferencing
- Professional video processing
- High-end consumer applications

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PNX1005E	BGA420	<tbd> **Remark:** Package currently is under qualification	SOT1136-1

5. Block diagram



Showing the maximum configuration of the multifunctional GPIO interface. Not all choices may be possible at the same time (see Section 8.1).

Fig 1. Block diagram of PNX1005

6. Pinning information

6.1 Pinning

Remark: Package SOT1136-1 currently is under qualification

Fig 2. Pin configuration for BGA420

Table 2. Pin allocation table[1][2]

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
A1	V_{SS}	A2	V_{SS}	A3	$V_{DDD(IO)(DDR)}$	A4	MM_DS_N0
A5	$V_{DDD(IO)(DDR)}$	A6	MM_DM0	A7	MM_D11	A8	$V_{DDD(IO)(DDR)}$
A9	MM_BA1	A10	$V_{DDA(DLL1)}$	A11	$V_{DDD(IO)(DDR)}$	A12	MM_A1
A13	$V_{DDD(IO)(DDR)}$	A14	MM_A4	A15	MM_CLK_P	A16	$V_{DDD(IO)(DDR)}$
A17	MM_PVT	A18	MM_D18	A19	MM_DS_P2	A20	$V_{DDD(IO)(DDR)}$
A21	MM_DS_P3	A22	V_{SS}	-	-	-	-
Row B							
B1	V_{SS}	B2	V_{SS}	B3	V_{SS}	B4	MM_DS_P0
B5	V_{SS}	B6	$V_{DDA(DLL0)}$	B7	MM_D7	B8	MM_D14
B9	MM_BA0	B10	$V_{SSA(DLL1)}$	B11	MM_A0	B12	MM_A5
B13	MM_A3	B14	MM_VREF	B15	MM_CLK_N	B16	V_{SS}
B17	MM_RAS_N	B18	MM_D19	B19	MM_DS_N2	B20	V_{SS}
B21	MM_DS_N3	B22	MM_D30	-	-	-	-
Row C							
C1	$V_{DDD(IO)}$	C2	VDI_D0	C3	MM_D0	C4	V_{SS}
C5	MM_D1	C6	V_{SS}	C7	$V_{SSA(DLL0)}$	C8	V_{SS}
C9	MM_D12	C10	V_{SS}	C11	MM_BA2	C12	V_{SS}
C13	MM_A10	C14	MM_A12	C15	MM_A13	C16	MM_CS_N
C17	$V_{DDD(IO)(DDR)}$	C18	MM_D23	C19	$V_{DDD(IO)(DDR)}$	C20	MM_D22
C21	$V_{DDD(IO)(DDR)}$	C22	MM_D31	-	-	-	-
Row D							
D1	CLKOUT	D2	VDI_D6	D3	V_{SS}	D4	$V_{DDD(IO)(DDR)}$
D5	MM_D2	D6	MM_D3	D7	MM_D5	D8	MM_D8
D9	MM_D13	D10	MM_DS_N1	D11	MM_A6	D12	MM_A8
D13	MM_CAS_N	D14	$V_{SSA(DLL2)}$	D15	MM_WE_N	D16	V_{SS}
D17	MM_D20	D18	V_{SS}	D19	V_{SS}	D20	MM_D29
D21	VDO_D2	D22	VDO_D6	-	-	-	-
Row E							
E1	GPIO14	E2	$V_{DDD(IO)}$	E3	VDI_D7	E4	VDI_D4
E5	VDI_D3	E6	VDI_D1	E7	MM_D4	E8	MM_DM1
E9	MM_D9	E10	MM_DS_P1	E11	V_{SS}	E12	MM_A7
E13	MM_CKE	E14	$V_{DDA(DLL2)}$	E15	MM_D17	E16	$V_{DDD(IO)(DDR)}$

Table 2. Pin allocation table[1][2] *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
E17	$V_{DDD(IO)(DDR)}$	E18	MM_DM2	E19	MM_DM3	E20	V_{SS}
E21	VDO_D7	E22	VDO_D12	-	-	-	-
Row F							
F1	VDI_D13	F2	VDI_D10	F3	V_{SS}	F4	$V_{DDA(DDR/PLL)}$
F5	VDI_D5	F6	VDI_D2	F7	MM_D6	F8	V_{SS}
F9	MM_D10	F10	MM_D15	F11	MM_A2	F12	MM_A9
F13	MM_A11	F14	MM_ODT	F15	MM_D16	F16	MM_D24
F17	MM_D21	F18	MM_D25	F19	MM_D27	F20	VDO_D4
F21	$V_{DDD(IO)}$	F22	VDO_D10	-	-	-	-
Row G							
G1	$V_{DDD(IO)}$	G2	VDI_D14	G3	VDI_D12	G4	GPIO15
G5	VDI_D8	G6	$V_{SSA(DDR/PLL)}$	G7	V_{SS}	G8	V_{SS}
G9	$V_{DDD(IO)(DDR)}$	G10	$V_{DDD(IO)(DDR)}$	G11	$V_{DDD(C)}$	G12	$V_{DDD(C)}$
G13	$V_{DDD(IO)(DDR)}$	G14	$V_{DDD(IO)(DDR)}$	G15	V_{SS}	G16	V_{SS}
G17	MM_D28	G18	MM_D26	G19	VDO_D0	G20	V_{SS}
G21	VDO_D13	G22	VDO_D16	-	-	-	-
Row H							
H1	GPIO11	H2	GPIO10	H3	V_{SS}	H4	VDI_CLK1
H5	VDI_D9	H6	GPIO38	H7	$V_{DDD(C)}$	H16	$V_{DDD(C)}$
H17	V_{SS}	H18	VDO_D3	H19	VDO_D5	H20	VDO_D9
H21	VDO_D17	H22	$V_{DDD(IO)}$	-	-	-	-
Row J							
J1	GPIO12	J2	$V_{DDD(IO)}$	J3	V_{SS}	J4	GPIO34
J5	VDI_D15	J6	VDI_D11	J7	$V_{DDD(C)}$	J16	$V_{DDD(C)}$
J17	VDO_D1	J18	VDO_D8	J19	VDO_D11	J20	V_{SS}
J21	VDO_D19	J22	VDO_D22	-	-	-	-
Row K							
K1	GPIO13	K2	VDI_CLK0	K3	V_{SS}	K4	GPIO33
K5	GPIO31	K6	GPIO32	K7	$V_{DDD(IO)}$	K16	$V_{DDD(IO)}$
K17	VDO_D18	K18	VDO_D15	K19	VDO_D14	K20	VDO_CLK
K21	$V_{DDD(IO)}$	K22	VDO_D24	-	-	-	-
Row L							
L1	$V_{DDD(IO)}$	L2	VDI_CLK2	L3	GPIO27	L4	GPIO28
L5	GPIO29	L6	GPIO30	L7	$V_{DDD(IO)}$	L16	$V_{DDD(IO)}$
L17	VDO_D23	L18	VDO_D21	L19	VDO_D20	L20	V_{SS}
L21	VDO_D25	L22	VDO_D26	-	-	-	-
Row M							
M1	GPIO17	M2	GPIO39	M3	$V_{SSA(CGU/PLL)}$	M4	V_{SS}
M5	$V_{SSA(OSC)}$	M6	$V_{SSA(CAB/DDS)}$	M7	V_{SS}	M16	V_{SS}
M17	VDO_D33	M18	VDO_D30	M19	VDO_D29	M20	VDO_D28
M21	VDO_D27	M22	$V_{DDD(IO)}$	-	-	-	-

Table 2. Pin allocation table[1][2] *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row N							
N1	$V_{DDA(CGU/PLL)}$	N2	$V_{DDA(OSC)}$	N3	V_{SS}	N4	$V_{DDA(CAB)(1V2)}$
N5	$V_{SSA(CAB)}$	N6	$V_{SSA(CAB/DDS)}$	N7	$V_{DDD(C)}$	N16	$V_{DDD(C)}$
N17	SYS_RST_OUT_N	N18	VDO_AUX	N19	VDO_D35	N20	V_{SS}
N21	VDO_D32	N22	VDO_D31	-	-	-	-
Row P							
P1	XTAL_O	P2	$V_{DDA(CAB/DDS)}$	P3	V_{SS}	P4	$V_{SSA(CAB/DDS)}$
P5	GPIO49	P6	AO12_WS	P7	$V_{DDD(C)}$	P16	$V_{DDD(C)}$
P17	V_{SS}	P18	GPIO2	P19	GPIO1	P20	VDO_VER
P21	$V_{DDD(IO)}$	P22	VDO_D34	-	-	-	-
Row R							
R1	XTAL_I	R2	$V_{DDD(IO)}$	R3	n.c.	R4	GPIO51
R5	GPIO40	R6	GPIO41	R7	$V_{DDD(C)}$	R16	$V_{DDD(C)}$
R17	SCL	R18	SDA	R19	GPIO5	R20	V_{SS}
R21	GPIO0	R22	VDO_HOR	-	-	-	-
Row T							
T1	$V_{DDA(CAB/DDS)}$	T2	$V_{DDA(CAB)(3V3)}$	T3	V_{SS}	T4	GPIO44
T5	GPIO42	T6	GPIO43	T7	$V_{DDD(IO)}$	T8	V_{SS}
T9	$V_{DDD(C)}$	T10	V_{SS}	T11	$V_{DDD(C)}$	T12	$V_{DDD(C)}$
T13	V_{SS}	T14	$V_{DDD(C)}$	T15	V_{SS}	T16	$V_{DDD(IO)(PCI)}$
T17	GPIO55	T18	V_{SS}	T19	RESET_IN_N	T20	GPIO6
T21	GPIO3	T22	$V_{DDD(IO)}$	-	-	-	-
Row U							
U1	$V_{DDD(IO)}$	U2	n.c.	U3	AO12_OSCLK	U4	GPIO46
U5	$V_{SSA(TERM)(USB)}$	U6	$V_{DDA(DRV)(USB)}$	U7	USB_RPU	U8	GPIO60
U9	V_{SS}	U10	$V_{DDD(IO)(PCI)}$	U11	V_{SS}	U12	V_{SS}
U13	$V_{DDD(IO)(PCI)}$	U14	V_{SS}	U15	PCI_AD2	U16	GPIO19
U17	GPIO57	U18	GPIO54	U19	TMS	U20	V_{SS}
U21	GPIO7	U22	GPIO4	-	-	-	-
Row V							
V1	GPIO50	V2	AO12_BCK	V3	V_{SS}	V4	USB_VBUS
V5	$V_{DDA(USB)}$	V6	USB_RREF	V7	GPIO18	V8	PCI_INTA_N
V9	PCI_AD23	V10	PCI_AD19	V11	PCI_AD16	V12	PCI_STOP_N
V13	GPIO36	V14	PCI_AD8	V15	GPIO35	V16	GPIO23
V17	GPIO56	V18	GPIO58	V19	GPIO53	V20	TDO
V21	$V_{DDD(IO)(PCI)}$	V22	POR_IN_N	-	-	-	-
Row W							
W1	GPIO52	W2	$V_{DDD(IO)}$	W3	$V_{SSA(REF)(USB)}$	W4	$V_{SSA(USB)}$
W5	USB_ID	W6	PCI_SYS_CLK	W7	PCI_AD27	W8	PCI_AD26
W9	PCI_IDSEL	W10	PCI_AD18	W11	PCI_TRDY_N	W12	PCI_SERR_N
W13	PCI_PAR	W14	PCI_AD12	W15	PCI_AD5	W16	PCI_AD3

Table 2. Pin allocation table[1][2] *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
W17	GPIO24	W18	GPIO22	W19	GPIO20	W20	V_{SS}
W21	TDI	W22	TCK	-	-	-	-
Row Y							
Y1	GPIO45	Y2	GPIO9	Y3	V_{SS}	Y4	GPIO48
Y5	V_{SS}	Y6	PCI_AD28	Y7	V_{SS}	Y8	PCI_AD25
Y9	V_{SS}	Y10	PCI_AD17	Y11	V_{SS}	Y12	PCI_AD14
Y13	V_{SS}	Y14	PCI_AD15	Y15	V_{SS}	Y16	PCI_AD9
Y17	PCI_AD6	Y18	GPIO26	Y19	V_{SS}	Y20	GPIO21
Y21	$V_{DDD(IO)(PCI)}$	Y22	V_{SS}	-	-	-	-
Row AA							
AA1	USB_DM	AA2	USB_DP	AA3	GPIO47	AA4	PCI_AD29
AA5	$V_{DDA(FB)(1V2)}$	AA6	PCI_AD24	AA7	PCI_CLK	AA8	PCI_AD20
AA9	PCI_AD21	AA10	PCI_DEVSEL_N	AA11	PCI_AD13	AA12	PCI_FRAME_N
AA13	PCI_AD7	AA14	PCI_AD10	AA15	PCI_AD0	AA16	PCI_AD11
AA17	PCI_CBE0_N	AA18	$V_{DDD(IO)(PCI)}$	AA19	V_{SS}	AA20	$V_{DDD(IO)(PCI)}$
AA21	GPIO8	AA22	GPIO16	-	-	-	-
Row AB							
AB1	V_{SS}	AB2	PCI_AD30	AB3	PCI_AD31	AB4	$V_{DDD(IO)(PCI)}$
AB5	PCI_CBE3_N	AB6	$V_{DDD(IO)(PCI)}$	AB7	PCI_AD22	AB8	$V_{DDD(IO)(PCI)}$
AB9	PCI_IRDY_N	AB10	$V_{DDD(IO)(PCI)}$	AB11	PCI_SERR_N	AB12	$V_{DDD(IO)(PCI)}$
AB13	PCI_CBE2_N	AB14	$V_{DDD(IO)(PCI)}$	AB15	PCI_CBE1_N	AB16	PCI_AD1
AB17	$V_{DDD(IO)(PCI)}$	AB18	PCI_AD4	AB19	GPIO59	AB20	GPIO37
AB21	GPIO25	AB22	V_{SS}	-	-	-	-

[1] See Section 8.1 for more functions available through the multiplexed GPIO interface and its default configuration. This interface extends functionality for digital video, extended I/O, host access, PCI-bus, USB-bus, digital audio, clocks and generic functions. Please keep in mind that some combinations may be mutually exclusive, depending on the specific application.

[2] n.c. indicate pins, which aren't connected internally to the die. Those pins have no electrical function.

6.2 Pin description

Table 3. Pin description overview

Pin category[1]	Table number
Power supply pins	Table 4
DDR SDRAM memory interface pins	Table 5
Digital video input interface pins	Table 6
Digital video output interface pins	Table 7
Digital audio interface pins	Table 8
Multifunctional GPIO interface pins	Table 9
PCI-bus interface pins	Table 10
USB-bus interface pins	Table 11
JTAG interface pins	Table 12
I^2C-bus interface pins	Table 13
Main control pins	Table 14
Crystal oscillator pins	Table 15
Not connected pins	Table 16

[1] See Section 8.1 for multiplexed GPIO functionality for video, XIO, host interface, PCI-bus, USB-bus, audio, clocks and generic functions.

Table 4. Pin description (power supplies)

Symbol	Pin	Type[1]	Description
Analog supply voltage pins			
$V_{DDA(CAB)(1V2)}$	N4	PS	CAB analog supply voltage (1.2 V)
$V_{DDA(CAB)(3V3)}$	T2	PS	CAB analog supply voltage (3.3 V)
$V_{DDA(CAB/DDS)}$	P2 and T1	PS	CAB/DDS analog supply voltage
$V_{DDA(CGU/PLL)}$	N1	PS	CGU/PLL analog supply voltage
$V_{DDA(DDR/PLL)}$	F4	PS	DDR/PLL analog supply voltage
$V_{DDA(DLL0)}$	B6	PS	DLL0 analog supply voltage
$V_{DDA(DLL1)}$	A10	PS	DLL1 analog supply voltage
$V_{DDA(DLL2)}$	E14	PS	DLL2 analog supply voltage
$V_{DDA(OSC)}$	N2	PS	oscillator analog supply voltage
$V_{DDA(DRV)(USB)}$	U6	PS	USB driver analog supply voltage
$V_{DDA(FB)(1V2)}$	AA5	PS	Fuse Box analog supply voltage (1.2 V)
$V_{DDA(USB)}$	V5	PS	USB analog supply voltage
Digital supply voltage pins			
$V_{DDD(C)}$	G11, G12, H7, H16, J7, J16, N7, N16, P7, P16, R7, R16, T9, T11, T12 and T14	PS	core digital supply voltage
$V_{DDD(IO)}$	C1, E2, F21, G1, H22, J2, K7, K16, K21, L1, L7, L16, M22, P21, R2, T7, T22, U1 and W2	PS	I/O digital supply voltage
$V_{DDD(IO)(DDR)}$	A3, A5, A8, A11, A13, A16, A20, C17, C19, C21, D4, E16, E17, G9, G10, G13 and G14	PS	DDR I/O digital supply voltage
$V_{DDD(IO)(PCI)}$	T16, U10, U13, V21, Y21, AA18, AA20, AB4, AB6, AB8, AB10, AB12, AB14 and AB17	PS	PCI I/O digital supply voltage[2]
Ground supply voltage pins			
V_{SS}	A1, A2, A22, B1, B2, B3, B5, B16, B20, C4, C6, C8, C10. C12, D3, D16, D18, D19, E11, E20, F3, F8, G7, G8, G15, G16, G20, H3, H17, J3, J20, K3, L20, M4, M7, M16, N3, N20, P3, P17, R20, T3, T8, T10, T13, T15, T18, U9, U11, U12, U14, U20, V3, W20, Y3, Y5, Y7, Y9, Y11, Y13, Y15, Y19, Y22, AA19, AB1 and AB22	G	ground supply voltage
$V_{SSA(CAB)}$	N5	G	CAB analog ground supply voltage
$V_{SSA(CAB/DDS)}$	M6, N6 and P4	G	CAB/DDS analog ground supply voltage
$V_{SSA(CGU/PLL)}$	M3	G	CGU/PLL analog ground supply voltage
$V_{SSA(DDR/PLL)}$	G6	G	DDR/PLL analog ground supply voltage
$V_{SSA(DLL0)}$	C7	G	DLL0 analog ground supply voltage
$V_{SSA(DLL1)}$	B10	G	DLL1 analog ground supply voltage
$V_{SSA(DLL2)}$	D14	G	DLL2 analog ground supply voltage
$V_{SSA(OSC)}$	M5	G	oscillator analog ground supply voltage

Table 4. Pin description (power supplies) *…continued*

Symbol	Pin	Type[1]	Description
$V_{SSA(REF)(USB)}$	W3	G	USB reference analog ground supply voltage
$V_{SSA(TERM)(USB)}$	U5	G	USB termination analog ground supply voltage
$V_{SSA(USB)}$	W4	G	USB analog ground supply voltage

[1] Table 17 defines the pin type.

[2] These pins are 5 V tolerant.

Table 5. Pin description (DDR SDRAM memory interface)

Symbol	Pin	Type[1]	Description
MM_A13	C15	A-O	address bit 13
MM_A12	C14	A-O	address bit 12
MM_A11	F13	A-O	address bit 11
MM_A10	C13	A-O	address bit 10
MM_A9	F12	A-O	address bit 9
MM_A8	D12	A-O	address bit 8
MM_A7	E12	A-O	address bit 7
MM_A6	D11	A-O	address bit 6
MM_A5	B12	A-O	address bit 5
MM_A4	A14	A-O	address bit 4
MM_A3	B13	A-O	address bit 3
MM_A2	F11	A-O	address bit 2
MM_A1	A12	A-O	address bit 1
MM_A0	B11	A-O	address bit 0
MM_BA2	C11	A-O	bank address bit 2
MM_BA1	A9	A-O	bank address bit 1
MM_BA0	B9	A-O	bank address bit 0
MM_CAS_N	D13	A-O	column address selector (active LOW)
MM_CKE	E13	AF-O	clock enable
MM_CLK_N	B15	C-O	negative clock
MM_CLK_P	A15	C-O	positive clock
MM_CS_N	C16	A-O	chip select (active LOW)
MM_D31	C22	D-IO	data bit 31
MM_D30	B22	D-IO	data bit 30
MM_D29	D20	D-IO	data bit 29
MM_D28	G17	D-IO	data bit 28
MM_D27	F19	D-IO	data bit 27
MM_D26	G18	D-IO	data bit 26
MM_D25	F18	D-IO	data bit 25
MM_D24	F16	D-IO	data bit 24
MM_D23	C18	D-IO	data bit 23
MM_D22	C20	D-IO	data bit 22
MM_D21	F17	D-IO	data bit 21

Table 5. Pin description (DDR SDRAM memory interface) *…continued*

Symbol	Pin	Type[1]	Description
MM_D20	D17	D-IO	data bit 20
MM_D19	B18	D-IO	data bit 19
MM_D18	A18	D-IO	data bit 18
MM_D17	E15	D-IO	data bit 17
MM_D16	F15	D-IO	data bit 16
MM_D15	F10	D-IO	data bit 15
MM_D14	B8	D-IO	data bit 14
MM_D13	D9	D-IO	data bit 13
MM_D12	C9	D-IO	data bit 12
MM_D11	A7	D-IO	data bit 11
MM_D10	F9	D-IO	data bit 10
MM_D9	E9	D-IO	data bit 9
MM_D8	D8	D-IO	data bit 8
MM_D7	B7	D-IO	data bit 7
MM_D6	F7	D-IO	data bit 6
MM_D5	D7	D-IO	data bit 5
MM_D4	E7	D-IO	data bit 4
MM_D3	D6	D-IO	data bit 3
MM_D2	D5	D-IO	data bit 2
MM_D1	C5	D-IO	data bit 1
MM_D0	C3	D-IO	data bit 0
MM_DM3	E19	A-O	data write enable for byte 3, i.e. MM_D[31:24]
MM_DM2	E18	A-O	data write enable for byte 2, i.e. MM_D[23:16]
MM_DM1	E8	A-O	data write enable for byte 1, i.e. MM_D[15:8]
MM_DM0	A6	A-O	data write enable for byte 0, i.e. MM_D[7:0]
MM_DS_N3	B21	R-IO	negative data strobe for byte 3, i.e. MM_D[31:24]
MM_DS_N2	B19	R-IO	negative data strobe for byte 2, i.e. MM_D[23:16]
MM_DS_N1	D10	R-IO	negative data strobe for byte 1, i.e. MM_D[15:8]
MM_DS_N0	A4	R-IO	negative data strobe for byte 0, i.e. MM_D[7:0]
MM_DS_P3	A21	R-IO	positive data strobe for byte 3, i.e. MM_D[31:24]
MM_DS_P2	A19	R-IO	positive data strobe for byte 2, i.e. MM_D[23:16]
MM_DS_P1	E10	R-IO	positive data strobe for byte 1, i.e. MM_D[15:8]
MM_DS_P0	B4	R-IO	positive data strobe for byte 0, i.e. MM_D[7:0]
MM_ODT	F14	AF-O	on-die termination
MM_PVT	A17	AR	process voltage temperature compensation
MM_RAS_N	B17	A-O	row address selector (active LOW)
MM_VREF	B14	AI	reference voltage[2]
MM_WE_N	D15	A-O	write enable (active LOW)

[1] Table 17 defines the pin type.

[2] Connect to $V_{DDD(IO)(DDR)}$ through a 130 Ω ± 1 % voltage divider.

Table 6. Pin description (digital video input interface)[1]

Symbol	Pin	Type[2]	Description
VDI_CLK2	L2	H-IO	clock 2
VDI_CLK1	H4	H-IO	clock 1
VDI_CLK0	K2	H-IO, H-OZ	clock 0
VDI_D15	J5	F-I	data bit 15
VDI_D14	G2	F-I	data bit 14
VDI_D13	F1	F-I	data bit 13
VDI_D12	G3	F-I	data bit 12
VDI_D11	J6	F-I	data bit 11
VDI_D10	F2	F-I	data bit 10
VDI_D9	H5	F-I	data bit 9
VDI_D8	G5	F-I	data bit 8
VDI_D7	E3	F-I	data bit 7
VDI_D6	D2	F-I	data bit 6
VDI_D5	F5	F-I	data bit 5
VDI_D4	E4	F-I	data bit 4
VDI_D3	E5	F-I	data bit 3
VDI_D2	F6	F-I	data bit 2
VDI_D1	E6	F-I	data bit 1
VDI_D0	C2	F-I	data bit 0

[1] See Section 8.1 for more digital video input functions available through the multiplexed GPIO interface.

[2] Table 17 defines the pin type.

Table 7. Pin description (digital video output interface)[1]

Symbol	Pin	Type[2]	Description
VDO_AUX	N18	F-OZ	auxiliary video output
VDO_CLK	K20	H-IO	video clock input and output
VDO_D35	N19	F-OZ	data bit 35
VDO_D34	P22	F-OZ	data bit 34
VDO_D33	M17	F-OZ	data bit 33
VDO_D32	N21	F-OZ	data bit 32
VDO_D31	N22	F-OZ	data bit 31
VDO_D30	M18	F-OZ	data bit 30
VDO_D29	M19	F-OZ	data bit 29
VDO_D28	M20	F-OZ	data bit 28
VDO_D27	M21	F-OZ	data bit 27
VDO_D26	L22	F-OZ	data bit 26
VDO_D25	L21	F-OZ	data bit 25
VDO_D24	K22	F-OZ	data bit 24
VDO_D23	L17	F-OZ	data bit 23
VDO_D22	J22	F-OZ	data bit 22

Table 7. Pin description (digital video output interface)[1] *…continued*

Symbol	Pin	Type[2]	Description
VDO_D21	L18	F-OZ	data bit 21
VDO_D20	L19	F-OZ	data bit 20
VDO_D19	J21	F-OZ	data bit 19
VDO_D18	K17	F-OZ	data bit 18
VDO_D17	H21	F-OZ	data bit 17
VDO_D16	G22	F-OZ	data bit 16
VDO_D15	K18	F-OZ	data bit 15
VDO_D14	K19	F-OZ	data bit 14
VDO_D13	G21	F-OZ	data bit 13
VDO_D12	E22	F-OZ	data bit 12
VDO_D11	J19	F-OZ	data bit 11
VDO_D10	F22	F-OZ	data bit 10
VDO_D9	H20	F-OZ	data bit 9
VDO_D8	J18	F-OZ	data bit 8
VDO_D7	E21	F-OZ	data bit 7
VDO_D6	D22	F-OZ	data bit 6
VDO_D5	H19	F-OZ	data bit 5
VDO_D4	F20	F-OZ	data bit 4
VDO_D3	H18	F-OZ	data bit 3
VDO_D2	D21	F-OZ	data bit 2
VDO_D1	J17	F-OZ	data bit 1
VDO_D0	G19	F-OZ	data bit 0
VDO_HOR	R22	F-OZ	horizontal synchronization
VDO_VER	P20	F-IO	vertical synchronization

[1] See Section 8.1 for more digital video output functions available through the multiplexed GPIO interface.

[2] Table 17 defines the pin type.

Table 8. Pin description (digital audio interface)[1]

Symbol	Pin	Type[2]	Description
AO12_BCK	V2	L-IO	audio bit clock
AO12_OSCLK	U3	L-OZ	audio oscillator clock
AO12_WS	P6	F-IO	audio word select

[1] See Section 8.1 for more digital audio functions available through the multiplexed GPIO interface.

[2] Table 17 defines the pin type.

Table 9. Pin description (multifunctional GPIO interface)[1]

Symbol	Pin	Type[2]	Description
GPIO60	U8	P-IO	general purpose input or output 60
GPIO59	AB19	P-I	general purpose input or output 59
GPIO58	V18	P-O	general purpose input or output 58
GPIO57	U17	P-O	general purpose input or output 57

Table 9. Pin description (multifunctional GPIO interface)[1] ...continued

Symbol	Pin	Type[2]	Description
GPIO56	V17	P-I	general purpose input or output 56
GPIO55	T17	P-O	general purpose input or output 55
GPIO54	U18	P-O	general purpose input or output 54
GPIO53	V19	P-O	general purpose input or output 53
GPIO52	W1	S-O	general purpose input or output 52
GPIO51	R4	S-O	general purpose input or output 51
GPIO50	V1	S-O	general purpose input or output 50
GPIO49	P5	S-O	general purpose input or output 49
GPIO48	Y4	T-O	general purpose input or output 48
GPIO47	AA3	T-I	general purpose input or output 47
GPIO46	U4	L-OZ	general purpose input or output 46
GPIO45	Y1	L-IO	general purpose input or output 45
GPIO44	T4	F-IO	general purpose input or output 44
GPIO43	T6	S-IO	general purpose input or output 43
GPIO42	T5	S-IO	general purpose input or output 42
GPIO41	R6	F-IO	general purpose input or output 41
GPIO40	R5	L-IO	general purpose input or output 40
GPIO39	M2	S-I, S-O	general purpose input or output 39
GPIO38	H6	S-I	general purpose input or output 38
GPIO37	AB20	P-I	general purpose input or output 37
GPIO36	V13	P-IO	general purpose input or output 36
GPIO35	V15	P-IO, P-I	general purpose input or output 35
GPIO34	J4	L-IO, L-I	general purpose input or output 34
GPIO33	K4	F-IO	general purpose input or output 33
GPIO32	K6	S-IO	general purpose input or output 32
GPIO31	K5	S-IO	general purpose input or output 31
GPIO30	L6	S-IO	general purpose input or output 30
GPIO29	L5	S-IO	general purpose input or output 29
GPIO28	L4	L-IO	general purpose input or output 28
GPIO27	L3	F-IO	general purpose input or output 27
GPIO26	Y18	T-IO	general purpose input or output 26
GPIO25	AB21	T-IO	general purpose input or output 25
GPIO24	W17	T-IO	general purpose input or output 24
GPIO23	V16	T-IO	general purpose input or output 23
GPIO22	W18	T-IO	general purpose input or output 22
GPIO21	Y20	T-IO	general purpose input or output 21
GPIO20	W19	T-IO	general purpose input or output 20
GPIO19	U16	T-IO	general purpose input or output 19
GPIO18	V7	P-IO	general purpose input or output 18
GPIO17	M1	S-IO	general purpose input or output 17
GPIO16	AA22	T-O, T-OD	general purpose input or output 16

Table 9. Pin description (multifunctional GPIO interface)[1] *…continued*

Symbol	Pin	Type[2]	Description
GPIO15	G4	S-I	general purpose input or output 15
GPIO14	E1	S-I	general purpose input or output 14
GPIO13	K1	S-O	general purpose input or output 13
GPIO12	J1	-IO, OZ	general purpose input or output 12
GPIO11	H1	L-O	general purpose input or output 11
GPIO10	H2	F-O	general purpose input or output 10
GPIO9	Y2	L-OZ	general purpose input or output 9
GPIO8	AA21	T-O, T-I	general purpose input or output 8
GPIO7	U21	T-IO, T-D	general purpose input or output 7
GPIO6	T20	F-IO, F-D	general purpose input or output 6
GPIO5	R19	F-IO, F-D	general purpose input or output 5
GPIO4	U22	F-IO, F-D	general purpose input or output 4
GPIO3	T21	F-IO, F-D	general purpose input or output 3
GPIO2	P18	F-IO, F-D	general purpose input or output 2
GPIO1	P19	F-IO, F-D	general purpose input or output 1
GPIO0	R21	F-IO, F-D	general purpose input or output 0

[1] See Section 8.1 for all functions and the default configuration of the multiplexed, multifunctional GPIO interface. GPIO[6:0] can be selecteds as clocks. Data may only appear at GPIO[60:0].

[2] Table 17 defines the pin type.

Table 10. Pin description (PCI-bus interface)[1]

Symbol	Pin	Type[2]	Description
PCI_AD31	AB3	P-IO	bit 31 of the PCI address and data bus
PCI_AD30	AB2	P-IO	bit 30 of the PCI address and data bus
PCI_AD29	AA4	P-IO	bit 29 of the PCI address and data bus
PCI_AD28	Y6	P-IO	bit 28 of the PCI address and data bus
PCI_AD27	W7	P-IO	bit 27 of the PCI address and data bus
PCI_AD26	W8	P-IO	bit 26 of the PCI address and data bus
PCI_AD25	Y8	P-IO	bit 25 of the PCI address and data bus
PCI_AD24	AA6	P-IO	bit 24 of the PCI address and data bus
PCI_AD23	V9	P-IO	bit 23 of the PCI address and data bus
PCI_AD22	AB7	P-IO	bit 22 of the PCI address and data bus
PCI_AD21	AA9	P-IO	bit 21 of the PCI address and data bus
PCI_AD20	AA8	P-IO	bit 20 of the PCI address and data bus
PCI_AD19	V10	P-IO	bit 19 of the PCI address and data bus
PCI_AD18	W10	P-IO	bit 18 of the PCI address and data bus
PCI_AD17	Y10	P-IO	bit 17 of the PCI address and data bus
PCI_AD16	V11	P-IO	bit 16 of the PCI address and data bus
PCI_AD15	Y14	P-IO	bit 15 of the PCI address and data bus
PCI_AD14	Y12	P-IO	bit 14 of the PCI address and data bus
PCI_AD13	AA11	P-IO	bit 13 of the PCI address and data bus

Table 10. Pin description (PCI-bus interface)[1] *…continued*

Symbol	Pin	Type[2]	Description
PCI_AD12	W14	P-IO	bit 12 of the PCI address and data bus
PCI_AD11	AA16	P-IO	bit 11 of the PCI address and data bus
PCI_AD10	AA14	P-IO	bit 10 of the PCI address and data bus
PCI_AD9	Y16	P-IO	bit 9 of the PCI address and data bus
PCI_AD8	V14	P-IO	bit 8 of the PCI address and data bus
PCI_AD7	AA13	P-IO	bit 7 of the PCI address and data bus
PCI_AD6	Y17	P-IO	bit 6 of the PCI address and data bus
PCI_AD5	W15	P-IO	bit 5 of the PCI address and data bus
PCI_AD4	AB18	P-IO	bit 4 of the PCI address and data bus
PCI_AD3	W16	P-IO	bit 3 of the PCI address and data bus
PCI_AD2	U15	P-IO	bit 2 of the PCI address and data bus
PCI_AD1	AB16	P-IO	bit 1 of the PCI address and data bus
PCI_AD0	AA15	P-IO	bit 0 of the PCI address and data bus
PCI_CBE3_N	AB5	P-IO	bus command and byte enable 3 of the PCI-bus interface (active LOW)
PCI_CBE2_N	AB13	P-IO	bus command and byte enable 2 of the PCI-bus interface (active LOW)
PCI_CBE1_N	AB15	P-IO	bus command and byte enable 1 of the PCI-bus interface (active LOW)
PCI_CBE0_N	AA17	P-IO	bus command and byte enable 0 of the PCI-bus interface (active LOW)
PCI_CLK	AA7	P-I	clock signal of the PCI-bus interface
PCI_DEVSEL_N	AA10	P-I	device select signal of the PCI-bus interface (active LOW)
PCI_FRAME_N	AA12	P-I	frame signal of the PCI-bus interface (active LOW)
PCI_IDSEL	W9	P-I	initialization device select signal of the PCI-bus interface
PCI_INTA_N	V8	P-I, P-OD	interrupt signal of the PCI-bus interface (active LOW)
PCI_IRDY_N	AB9	P-IO	initiator ready signal of the PCI-bus interface (active LOW)
PCI_PAR	W13	P-IO	parity signal of the PCI-bus interface
PCI_PERR_N	W12	P-IO	parity error signal of the PCI-bus interface (active LOW)
PCI_SERR_N	AB11	P-OD	system error signal of the PCI-bus interface (active LOW)
PCI_STOP_N	V12	P-IO	stop signal of the PCI-bus interface (active LOW)
PCI_SYS_CLK	W6	P-IO	system clock signal of the PCI-bus interface
PCI_TRDY_N	W11	P-IO	target ready signal of the PCI-bus interface (active LOW)

[1] See Section 8.1 for more PCI-bus functions available through the multiplexed GPIO interface.

[2] Table 17 defines the pin type.

Table 11. Pin description (USB-bus interface)[1]

Symbol	Pin	Type[2]	Description
USB_DM	AA1	U-IO	minus data input and output of the USB-bus interface
USB_DP	AA2	U-IO	positive data input and output of the USB-bus interface
USB_ID	W5	U-I	type identification input of the USB-bus interface
USB_RPU	U7	U-I	pull-up resistor of the USB-bus interface
USB_RREF	V6	U-IO	resistor reference of the USB-bus interface[3]
USB_VBUS	V4	U-IO	bus voltage of the USB-bus interface

[1] See Section 8.1 for more USB-bus functions available through the multiplexed GPIO interface.

[2] Table 17 defines the pin type.

[3] Connect through a 12 kΩ ± 1 % resistance to the analog ground plane, which connects to pin $V_{SSA(USB)}$.

Table 12. Pin description (JTAG interface)

Symbol	Pin	Type[1]	Description
TCK	W22	T-I	test clock input
TDI	W21	T-I	test serial data input
TDO	V20	L-OZ	test serial data output
TMS	U19	T-I	test mode select input

[1] Table 17 defines the pin type.

Table 13. Pin description (I²C-bus interface)

Symbol	Pin	Type[1]	Description
SCL	R17	I2-I, I2-OD	serial clock input and output
SDA	R18	I2-I, I2-OD	serial data input and output

[1] Table 17 defines the pin type.

Table 14. Pin description (main control pins)

Symbol	Pin	Type[1]	Description
CLKOUT	D1	H-IO	clock output
POR_IN_N	V22	T-I	power-on reset input (active LOW)
RESET_IN_N	T19	T-I	master reset input (active LOW)
SYS_RST_OUT_N	N17	H-O	system reset output (active LOW)

[1] Table 17 defines the pin type.

Table 15. Pin description (crystal oscillator pins)

Symbol	Pin	Type[1]	Description
XTAL_I	R1	AI	crystal oscillator analog input
XTAL_O	P1	AO	crystal oscillator analog output

[1] Table 17 defines the pin type.

Table 16. Pin description (not connected pins)

Symbol	Pin	Type	Description
n.c.	R3 and U2	-	not connected

Table 17. Pin type description

Pin types are either generic or a combination of type and function. Examples are AO and P-OD.

Type	Description
Generic	
AI	analog input pin
AO	analog output pin
AR	analog reference pin
G	ground pin
PS	power supply pin
Type	
A	Address pin
AF	Address pin with Forced low output during power-down
C	Clock pin
D	Data pin
F	Fast pin (1 ns slew rate)
H	High-speed clock pin
I2	I^2C-bus pin; 3.3 V signaling, 5 V tolerant
L	Low-speed clock pin
P	PCI Local Bus 2.2 specification compliant pin; 3.3 V signaling, 5 V tolerant
R	stRobe pin
S	Slow pin (3 ns slew rate)
T	5 V Tolerant input
U	5 V tolerant USB-bus pin
Function	
I	Input
O	Output
IO	Input and Output
I/O	Input or Output
I/OD	Input or Output with open Drain
I/O/D	Input or Output or open Drain output with input
OD	Open Drain output
OZ	Tri-state Output

7. Functional description

7.1 Digital video

7.1.1 Video input

The PNX1005 has a versatile ViDeo Input (VDI) module with a:

- Video Input Processor (VIP) for 8-bit, 10-bit, 16-bit or 20-bit YUV capture
- Fast General Purpose Interface (FGPI) for 8-bit, 16-bit or 24-bit capture.

See Section 8 for configuration examples of these multiplexed interfaces.

7.1.1.1 VIP

The PNX1005 includes a dedicated Video Input Processor (VIP) module accepting a wides range of different video formats. The VIP interface is composed of 24 data pins VDI_D[23:0], five control pins VDI_V[2:0], VDI_HOR, VDI_VER and three video input clock pins VDI[2:0]_CLK. The VIP captures 8-bit or 10-bit streaming digital video from a parallel interface port.

Two parallel Digital Video (DV) ports are connected to the input of the VIP. The digital video is provided in an *ITU-R 656* compliant format, in a VESA compliant format or in a format with explicit synchronization signals. Typically, the digital video is YUV 4 : 2 : 2 encoded. Additionally, support is provided for RGB Bayer encoded video. Although only two DV ports are connected to the VIP, it is capable of capturing up to 8 digital video streams in parallel. This can be achieved by utilizing digital video decoders that time-multiplex 4 digital video streams into one stream, utilizing only one single DV port.

The VIP provided functionality is divided into the following steps, from capture to writing the video streams into main memory:

- Generate video stream test pattern
- Capture streams on the DV ports
- Decode streams
- Windowing of video streams; this step generates both a primary and an auxillary video stream
- Simple horizontal scaling (half resolution); co-sited or interspersed sampling of video data
- Dithering, to support translation of 10-bit video into 8-bit video
- Writing the video stream to main memory; support is provided for packed, semi-planar and planar memory layouts and 2-bit, 8-bit, 10-bit and 16-bit video data.

Decoding streams includes demultiplexing of multiple time-multiplexed video streams on a single logical DV port, combining the streams of two logical DV ports into a single High-Definition (HD) video stream and video image extraction. This step also includes the extraction of ancillary data that may be encoded in video blanking regions.

The windowing, scaling, dithering and writing to main memory steps are performed on each of the 8 video streams, each of which may be composed of a primary video stream, an auxillary video stream and an anicillary stream.

7.1.1.2 FGPI

In addition to the VIP module the PNX1005 has a Fast General Purpose Input (FGPI) interface which shares the VDI pins. The FGPI module is a high-bandwidth input data channel. The FGPI packs four 8-bit samples, two 16-bit samples or one 32-bit sample of data into one 32-bit word, which is sent to main memory via DMA. 30-bit video input formats like RGB/YUV(4 : 4 : 4) can be cpatured using the FGPI.

The full bandwidth capabilities of FGPI are not used since there are only 24 data pins allocated to FGPI in the PNX1005 device.

The FGPI operates in two main modes, record capture or message passing:

- Can be used as a versatile interface with streaming data sources
- Can be used as a receiver port for inter-TriMedia unidirectional message passing
- Permits optional synchronization with external control signals like h-sync and v-sync to capture video data
- POptionally inserts timestamp information into packet sent to memory
- Optionally inserts information, like message or record length, into packet sent to memory
- Permits continuous data transfer using DMA transfers to two main memory buffers.

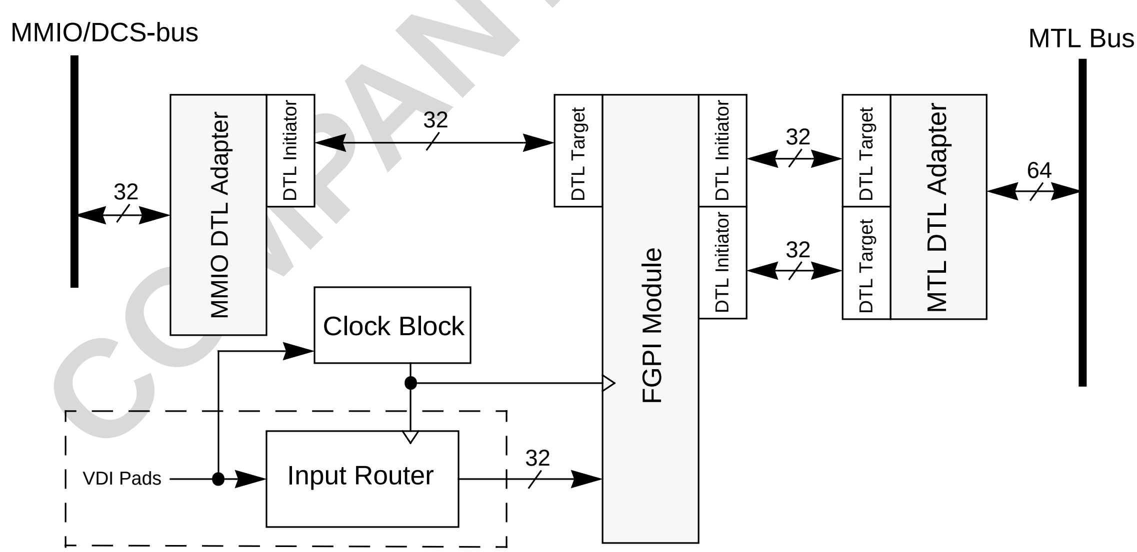


Fig 3. FPGI top level block diagram

7.1.2 Video output

The PNX1005 has a versatile ViDeo Output (VDO) module with a:

- DVD-Descrambler (DVD-D) module
- Quality video Composition Processor (QVCP) module
- Memory Based Scaler (MBS) module.

See Section 8 for configuration examples of these multiplexed interfaces.

The video output stream of the QVCP can be connected directly to the ViDeo Output (VDO) port VDO_D[35:0] of the PNX1005 in order to provide one video stream, but the PNX1005 can be used also to provide two different video streams to operate two LCD screens (i.e. for rear-seat entertainmant). Therefore the user can configure the QVCP to provide a multiplexed video output stream to the VDO buffer. The VDO buffer is used to demultiplex two combined video streams from the QVCP into two 18-bit RGB or two 24-bit RGB video output streams.

The PNX1005 has a ViDeo Out Buffer (VDOB) for 2 × 24-bit RGB output mode. For restrictions see Table 18.

7.1.2.1 DVD-D

The PNX1005 provides Digital Versatile Disc-Descrambler (DVD-D) module providing the major processes:

- Authentiction process
- Key conversion process
- Main data descrambling process.

A DVD player system consists then of a DVD-ROM drive which accepts the DVD-ROM disc and reads the information from the disc to the drive controller. The drive controller connects the disc transport with an interconnecting bus (PCI-XIO) and hence to the host system (PNX1005). The host system interacts with the DVDD module to send authorization requests, receive authorization, replies, and transfer data between the DVD-ROM Drive and the DVDD module.

7.1.2.2 QVCP

The Quality video Composition Processor (QVCP) module is a high-resolution image composition and processing pipeline that facilitates both graphics and video processing. In combination with several other modules, it provides a new generation of graphics and video capability. QVCP provides its advanced functionality using a series of layers and mixers; a series of display-data layers (pixel streams) are created and logically mixed in sequence to render the composite output picture.

The QVCP module contains a total number of two layers and is mainly intended to be connected to a TV, a monitor or LCD panel. Due to the independence of the layers, a number of different scenarios is possible. However, in general, the QVCP has been designed to mix one video plane and one graphic plane. It can therefore be used to display a fully composited video image consisting of graphical information, lik ePIP or menu.

QVCP supports a whole range of progressive and interlaced display standards: for televisions, from standard-definition resolutions such as PAL or NTSC to all eighteen ATSC display formats such as 1080i or 720p, and for computer and LCD displays at 60 Hz and up to 1080p resolutions. The wide variety of output modes guarantees the compatibility with most present display-processor chips.

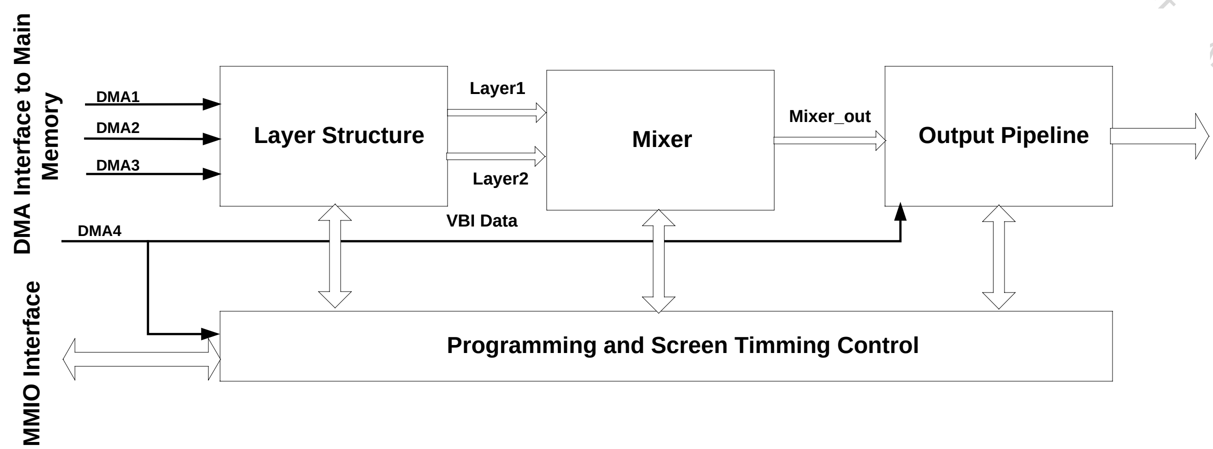


Fig 4. QVCP top level block diagram

In order to achieve high-quality video and graphics as demanded by future consumer products, a number of complex tasks need to be performed by the QVCP. The main functions of the video and graphics output pipeline are:

- Fetching of up to two video streams from memory
- Color expansion in case of non-full color or indexed data formats
- Reverse-gamma correction
- Video quality enhancement such as luminance sharpening, chroma transient improvement, histogram modification, skin-tone correction, blue stretch, and green enhancement
- Horizontal up-scaling for video and graphics images in both linear and panorama mode
- Adapting screen timing generation to the connected display requirements (SDTV standards, HDTV standards, progressive and interlaced formats)
- Color space uniqueness of all video streams
- Merging of thevideo streams (blend, invert and exchange)
- Positioning of the various video streams (including finer positioning)
- Brightness and contrast control on a for each video output stream
- Gamma correction and noise shaping of the final composited image
- Output format generation.

7.1.2.3 MBS

The captured data of the the VIP and the FPGI will get stored in main memory in the user defined address spaces. In order to enlarge or reduce the captured video images the PNX1005 has a Memory Based Scaler (MBS). Memory based scaling is done independent of any video clocks by reading the video data from memory and writing the scaled pictures back to the memory. A single scaler can therefore be used to scale more than one video stream sequentially.

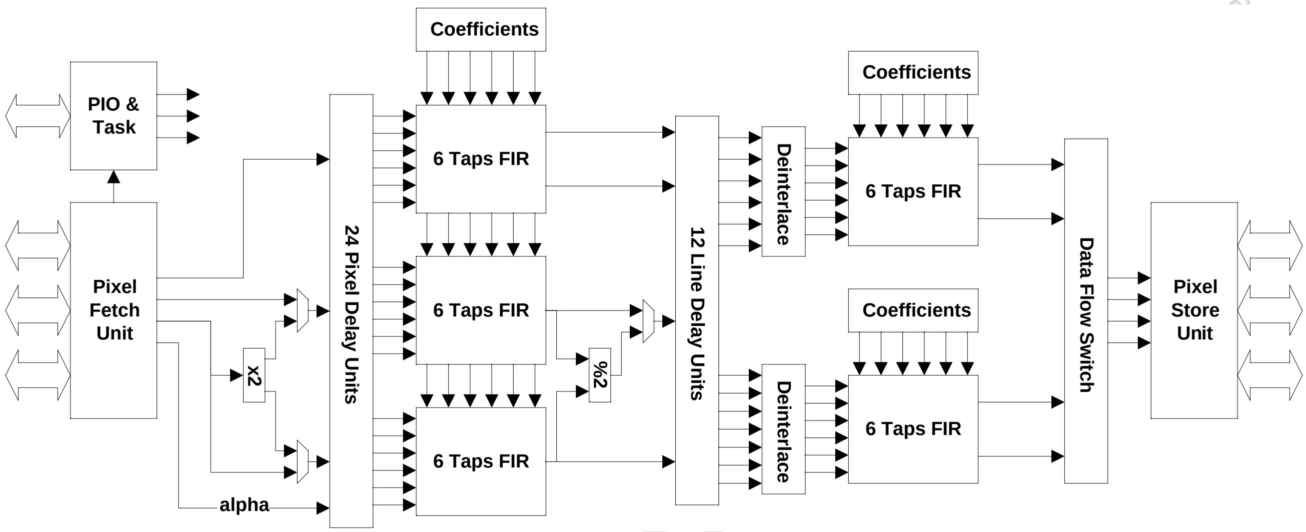


Fig 5. MBS block diagram

The memory-based scaler can perform the following operations:

- Vertical and horizontal scaling
  – Linear and non-linear aspect-ratio conversion (panorama scaling)
- De-interlacing
  – Simple median
  – Majority-selection (median filtering with previous field, spatial temporal average of 2 fields, same position from next or previous field depending on whether three or two field majority selection)

    Remark: Majority selection is done on luma only
  – Field insertion and line doubling (i.e., repeating the same line twice)
  – Edge-Dependent De-interlacing (EDDI), a post-processing step done on luma only
- Anti-flicker filtering
- Conversions between 4 : 2 : 0, 4 : 2 : 2 and 4 : 4 : 4
- Indexed to true color conversion
- Color expansion and compression (different quantizations for color components, e.g. RGB565 to RGB32)
- Deplanarization and planarization
- Variable color space conversion with programmable matrix coefficients (mutually exclusive with horizontal scaling)
- Color-key and alpha processing
  – Conversion between color-key and alpha
  – Alpha scaling

- Measurements
  - Histogram measurement
  - Noise estimation
  - Blackbar detection
  - Blacklevel measurement
  - UV bandwidth measurement
  - Task list based programming.

Most of the above functions can be performed during a single pass, though the filter quality (length) may vary depending on the performed operations.

Special modes and features:

- Color key to alpha and alpha to color key conversion (color re-keying)
- Non-linear phase interpolation (phase LUT).

7.2 Digital audio

The PNX1005 has digital audio inputs and outputs:

- Audio Input 2 (AI2) for 8 channels and master of the synchronization
- Audio Output 2 (AO2) for 8 channels and master of the synchronization.

For restrictions see Table 18 and Section 7.1.1.

7.2.1 Audio input

The PNX1005 device has an Audio Input (AI) module to receive digital audio input streams.

The AI module can activate up to four audio input ports. Each audio input port processes single-channel or dual-channel sources. Hence the AI module can capture up to 8 channels of audio input (4 stereo channels).

The AI module includes four major subsystems: a programmable sample clock generator, a serial-to-parallel converter, a Device Transaction Level (DTL) initiator interface that initiates transfer of parallel data to a DTL-to-memory bus adapter and a MMIO type low latency DTL target interface for MMIO configuration registers.

The sampling clock can be used as either master or slave to the external audio. The sampling clock synchronizes the serial-to-parallel converter with the source data stream. The samples enter the serial-to-parallel converter, which reformats the data for the initiator. The initiator streams the parallel data in to the DTL-to-memory bus adapter.

The AI module provides a DMA-driven serial interface to an off-chip stereo Analog-to-Digital Converter (ADC), I^2S subsystem or other serial data source. AI provides all signals needed to connect to high-quality, low-cost oversampling ADCs. The AI module and external ADC (or I^2S subsystem) together are capable of generating a programmable sample clock by dividing a precise oversampling clock, which will be provided by the internal clock factory of the PNX1005.

The AI module has the following features:

- Four channels of audio input per port
- 16-bit or 32-bit samples per channel
- Programmable 1 Hz to 192 kHz sampling rate

  Remark: This is a practical range; the actual sample rate is application dependent
- Internal or external sampling clock source
- AI autonomously writes sampled audio data to memory using the internal DMA network
- 16-bit and 32-bit mono and stereo PC standard memory data formats
- Raw mode where the bits from all the active inputs are sampled by bit clock along with the frame sync signal (pin AI1_WS or AI2_WS) and stored in memory
- Little-endian or big-endian memory formats.

Remark: AC-97 codecs are not supported.

The PNX1005 includes 2 identical AI modules. The pins available may however differ depending on the PNX1005 configuration being used.

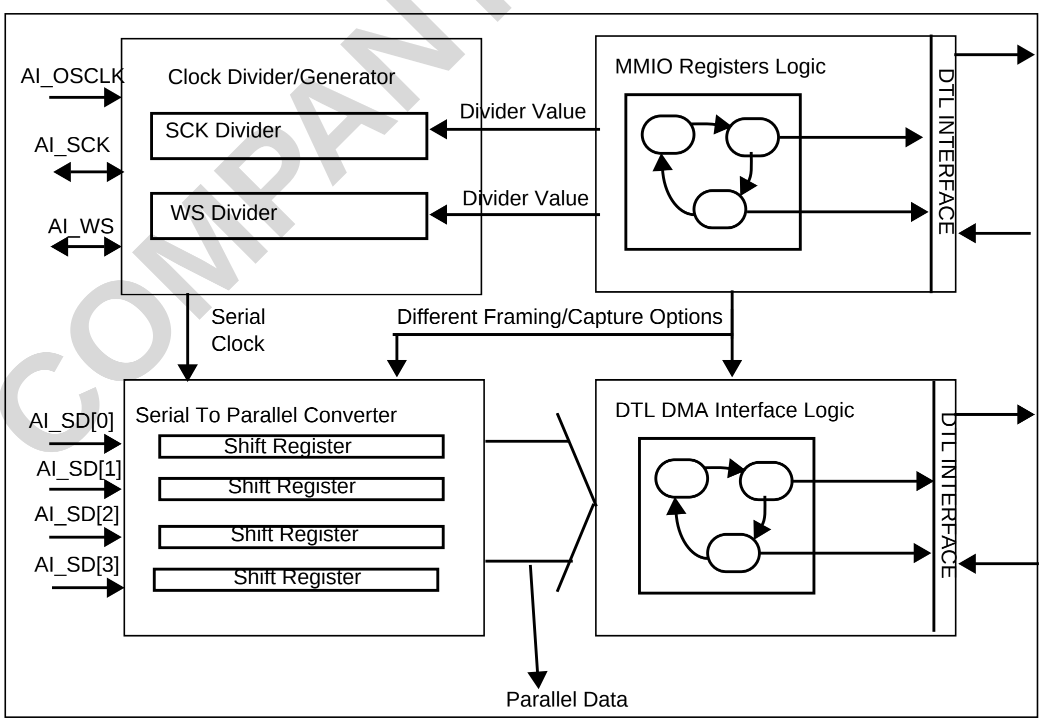


Fig 6. Audio in block diagram

7.2.2 Audio output

The PNX1005 device has an Audio Output (AO) module providing a DMA-driven serial interface designed to support stereo audio Digital-to-Analog Converters (DAC). The AO module can support up to eight PCM audio channels by driving up to four external stereo DACs. The AO module provides a direct connection interface to high-quality, low-cost oversampling DACs. A precise programmable oversampling clock is featured.

The AO module has four major subsystems: a programmable sample clock generator, a DMA engine, a parallel to serial converter and memory mapped registers for configuration and control. The AO connectors provide the digital audio stream, clock and control signals to external D/A converters. A block diagram of AO is illustrated in Figure 7.

The AO module, along with the external DACs, has the following capabilities:

- Up to 8 channels of audio output
- 16-bit or 32-bit samples per channel
- Programmable 1 Hz to 192 kHz sampling rate

  Remark: This is a practical range; the actual sample rate is application dependent
- Internal or external bit clock source
- Autonomously retrieves processed audio data from dual DMA buffers in memory
- 16-bit mono and stereo PC standard memory data formats
- Control capability for highly integrated PC codecs.

Remark: AC-97 codecs are not supported.

The DMA engine reads 16-bit or 32-bit samples from memory using dual DMA buffers in memory. Software initially assigns two full sample buffers in memory containing an integral number of samples for all active channels. The DMA engine retrieves samples from the first buffer in memory until exhausted and continues from the second buffer in memory as a request for a new first sample buffer in memory is issued to the system controller. This is a continuous process.

The samples are given to the data serializer (parallel-to-serial converter), which sends them out in a MSB first or LSB first serial frame format that can also contain one or two codec control words of up to 16 bits. The output frame structure is programmable.

PNX1005 includes 2 identical AO modules. The pins available may however differ depending on the PNX1005 configuration being used.

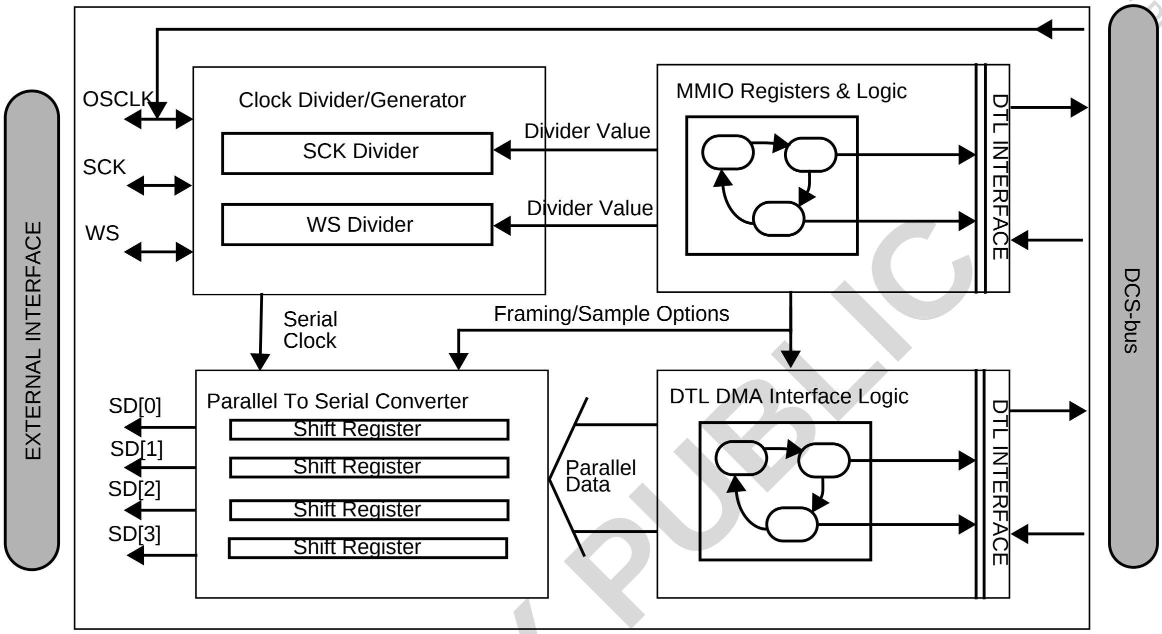


Fig 7. AO block diagram

7.3 Peripheral interfaces

7.3.1 DDR SDRAM memory interface

The DDR interface can operate in 32-bit or in 16-bit mode:

- 32-bit mode requires two $\times$ 16 DDR memory devices; maximum available bandwidth is 2.1 GB/s
- 16-bit mode requires only one $\times$ 16 DDR memory device; this option helps to reduce the Bill Of Materials (BOM), when one device alone satisfies the required system bandwidth, i.e. 1 GB/s.

7.3.2 DDR SDRAM memory interface

The PNX1005 has a DDR controller which is used to interface to off-chip DDR1 and DDR2 memory devices.

The primary features of the DDR SDRAM controller include:

- 16-bit or 32-bit wide data bus on DDR SDRAM memory side
- Three MTL ports (one for the DMA memory traffic, two for the CPU)
- Supports $\times$ 8 and $\times$ 16, 4 and 8 banks memory devices
- Supports up to 2 Gb DDR SDRAM memory devices
- Supports 1 rank (physical banks) of memory devices
- Maximum of 8 open pages for a maximum address range of 256 MB
- Halt modes and clock gating for power consumption reduction

- Programmable DDR SDRAM timing parameters that support different DDR SDRAM memory devices up to 266 MHz, i.e. 533 MHz data rate
- Programmable bank mapping scheme to potentially improve bandwidth utilization
- Programmable arbitration with latency or deadline guarantees with built-in performance monitors
- JEDEC compliant limited to burst length of 8.

The DDR controller module includes an arbiter which arbitrates between the DDR burst commands coming from the three different MTL ports. After arbitration, the DDR burst command selected by the arbiter is stored in a FIFO with 5 entries. The DDR module has a refresh counter to keep track of the refresh timing. The DDR module keeps track of the open pages in the DDR memories. The DDR command generator decides upon which command (refresh, precharge, activate, read or write) to generate based on the information in the FIFO with 5 entries, the state of the refresh counter, and the state of the DDR memories as indicated by the open page table.

7.3.3 Multifunctional GPIO interface

The PNX1005 has a 61-bit wide GPIO interface, which multiplexes various functions.

7.3.3.1 GPIO

The PNX1005 has 61 pins that are capable of operating as software controlled General Purpose Input Output (GPIO) pins. Eight of them are dedicated GPIO pins. The other 53 pins are assigned to the other PNX1005 modules, like the AO module, but they can be re-used as GPIO pins, see Section 8.1. So these are designated as optional GPIO pins that can either operate in regular mode or in GPIO mode. All 61 pins have common features:

- Software I/O, which sets a pin or pin group, enables a pin or a pin group and inspects pin values
- Precise timestamping of internal and external events (up to 12 signals simultaneously)
- Signal event sequence monitoring or signal generation (up to 4 signals simultaneously)
- Timer source selection for TM3282.

The 61 pins have the same GPIO capabilities. However some of the dedicated GPIO pins have additional features like:

- Clocks: these pins are possible clock source for pattern generation or sampling mode or they are simply used to provide a clock to peripherals on the PNX1005 system board
- Wake-up event: used to wake-up PNX1005 from deep-sleep mode
- Boot option: determines the boot settings of PNX1005
- Watchdog: this is a subset of the software I/O mode since the TM3282 CPU would toggle this pin at regular intervals in order to prevent an external watchdog to reset the entire system; alternately the internal watchdog timer of PNX1005 system can be used.

After a PNX1005 system reset has occured all the GPIO pins are set to GPIO mode and in input mode (tri-state).

A simplified block diagram of the GPIO module can be found in Figure 8. It presents the major interfaces of the GPIO module:

- The GPIO pins
- The MTL interface used to fetch data when operating in pattern generation mode or used to store data when the GPIO module is used in sampling mode.; in both cases up to 4 FIFO memory buffers are available for one of the modes
- The DCS-bus interface used to convey the MMIO register read and writes issued by the TM3282 CPU or any other master connected to PNX1005 through the PCI-bus interface
- The 5 interrupt lines which are routed directly to the TM3282 CPU; 4 lines are associated with the signal monitoring while the last interrupt line is linked to the event monitoring.

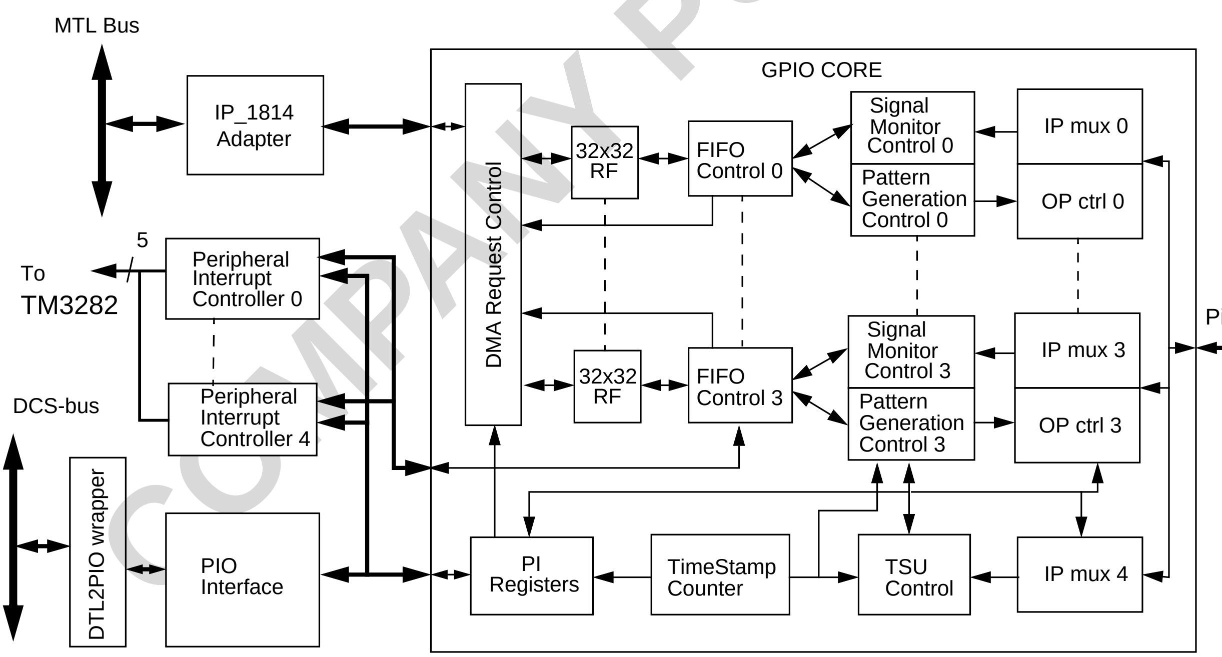


Fig 8. GPIO module block diagram

7.3.3.2 PCI-bus and XIO interface

The arbiter can control up to three external PCI masters, when the host interface is not used (see Table 18).

The XIO interface accepts up to five chip select signals and up to 16 data pins, when the host interface is not used (see Table 18).

For a full featured list of all PCI 2.2 configurations please contact NXP; see Section 20.

7.3.3.3 PCI-bus interface

PNX1005 includes a PCI-bus interface for easy integration into personal computer applications (where the PCI-bus is the standard for high-speed peripherals). In embedded applications the PCI-bus can interface to peripheral devices that implement functions not provided by the on-chip modules or to connected several CPUs together.

The PCI-XIO module supports 33 MHz and 66 MHz according to *PCI specification version 2.2*. It can operate as a configuration manager or it can also act as a target to external configuration cycles when an external processor and north bridge are used in the system.

Features:

- Three base addresses, i.e. apertures, are supported: DRAM, MMIO and XIO
- Option to enable internal PCI system arbiter which can support up to three external PCI masters
- As a PCI master, it can generate all non-reserved types of single transaction PCI cycles: I/O, memory, interrupt acknowledge and configuration cycle
- Linear burst mode is supported on memory transactions; other burst mode transfers are terminated after a single data transfer
- A DMA engine provides high-speed transfer to and from SDRAM and an external PCI device; the DMA can also be used to transfer data to and from XIO devices
- The PCI clock (at pin PCI_SYS_CLK) and PCI_RST_N (at pin RESET_IN_N) are generated externally and input to this module
- In PCI terminology it is a single function device.

The following general PCI-bus features are not implemented in the PCI-XIO module:

- As a PCI target, the device only responds to memory and configuration cycles
- Subtractive decoding is not supported
- There is no hard-coded legacy decoding of address space (such as VGA I/O and memory)
- Burst to configuration space is not supported.

The main function of the PCI-bus interface is to connect the PNX1005 on-chip MTL bus (and therefore its main memory) and its internal registers to external devices on the PCI-bus. A bus cycle on PCI that targets an address mapped into PNX1005 memory space will cause the PCI-bus interface to create a MTL bus cycle targeted at DRAM. From PNX1005, only the TM3282 CPU can cause the PCI-bus interface to create PCI-bus cycles; the other on-chip modules cannot access external hardware through the PCI-bus interface. From PCI, DRAM and most of the registers in MMIO space can be accessed by external PCI initiators.

The PCI-bus interface implements DMA (also called block or burst transfers) and non-DMA transfers. DMA transfers are interruptible on 64-byte boundaries.

The following classes of operations invoked by PNX1005 cause the PCI-bus interface to act as a PCI initiator:

- Transparent, single-word (or smaller) transactions caused by TM3282 loads and stores to one of the two available the PCI-bus address aperture, PCI1 and PCI2
- Explicitly programmed single-word I/O or configuration read or write transactions
- Explicitly programmed multi-word DMA transactions.

The PNX1005 PCI-bus interface responds as a target to external initiators for a limited set of PCI transaction types:

- Configuration R/W
- Memory R/W, read line, and read multiple to the PNX1005 DRAM or MMIO apertures.

PNX1005 ignores PCI transactions other than the above.

The PCI-XIO module also includes an XIO interface. Both interfaces don't execute simultaneously, see Table 18. The XIO interface uses PCI cycle to run XIO transfers before giving control back to PCI-bus. The XIO interface supports IDE, NAND and NOR type Flash and Motorola devices, in an 8-bit or 16-bit wide datapath. Maximum NAND FLASH supported per profile is 128 MB. Maximum NOR FLASH supported per profile is 128 MB. PCI-XIO supports up to 5 profiles.

7.3.3.4 USB-bus interface

An USB-bus interface on dedicated I/O pins have been implemented in the PNX1005 fulfilling the *USB 2.0 HS OTG specification*. USB 2.0 offers the user a larger bandwidth increasing data throughput by a factor of 40 compared to USB 1.1. All the peripherals used with the previous versions of USB work perfectly with USB 2.0 while also offering a larger choice of higher performance peripherals, such as video cameras, fast storages devices, GPS receiver, etc. In addition to the 1.5 Mb/s and 12 Mb/s data rates of USB 1.1, the evolution from USB 1.1 to USB 2.0 adds an additional data rate of 480 MB/s.

Additionaly the PNX1005 provides the OTG functionality of USB 2.0. The On-The-Go (OTG) supplement to the USB Specification extends USB to peer-to-peer application. Using USB OTG technology the PNX1005 can be directly connected to a storeage device or host to exchange data. The OTG state machines determine the role of the device based on connector signals, and then initializes the device in the appropriate mode of operation (host or peripheral) based on how it is connected. After connecting the devices can negotiate using the OTG protocols to assume the role of host or peripheral based on the task to be accomplished.

The USB-bus interface supports the USB 2.0 HS OTG standard. It has two optional LED pins at pins USB_LED[1:0]. For availability and restrictions see Table 18.

7.3.3.5 Host interface

Parts of the multiplexed GPIO interface can operate as the host interface. For effect on other PNX1005 features see Table 18.

The PNX1005 provides a high-speed interface for I^{2}C-bus communication with a host processor to exchange data as well as command messages. Two separated channels are implemented to ease the software development by providing separated data buffers in the PNX1005 for data and command messages. The command message structure can be defined freely by the user to adapt the PNX1005 to the target system. The data/command buffer sizes can be defined independent of each other from 16 byte to several kB or MB depending on the available main memmory space. The host interface can be used in transaction modes with a data width of 16-bit or 8-bit by providing data transfer rates of up to 400 Mb/s (16-bit mode) or 200 Mb/s (8-bit mode).

7.3.4 I^{2}C-bus interface

The PNX1005 has a 5 V tolerant standard I^{2}C-bus interface, which can work as slave or master on the bus configurable during run time. The PNX1005 can load the boot code via an external connected I^{2}C EEPROM after reset and switch into slave mode if an external master requests the I^{2}C-bus. The interface can run on 100 kHz as well as on 400 kHz.

7.3.5 JTAG interface

The PNX1005 has a dedicated JTAG interface for software development.

8. Application design-in information

8.1 Multiplexed GPIO functionality

The PNX1005 has a versatile, software programmable GPIO interface for enhanced video and multimedia functionality. Applications can use the GPIO interface for general purpose input and output. Table 18 lists extended functionality from the GPIO interface for:

- Digital video input functions
- Digital video output functions
- Digital audio functions
- Extended I/O functions
- Host interface functions
- PCI-bus functions extension
- USB-bus functions extension
- Clock signals
- Generic signals.

Remark: The PNX1005 uses the GPIOs in boot mode. After finishing the boot process the GPIOs are available for the multiplexed functions (see Table 18).

Remark: Please note that these multiplexed functions are mutually exclusive, i.e. they may not be available at the same time depending on the software enabled configuration of the PNX1005.

Remark: For default configuration of GPIO pins and functionality see Table 19.

Table 18. Multiplexed GPIO functionality[1]

GPIO pin	Interfaces with mutually exclusive functionality								
	Video input	Video output	Extended I/O	Host	PCI	USB	Audio[2]	Clocks	Generic
GPIO0	-	-	-	-	-	-	-	CLOCK0	BOOT_MODE0
GPIO1	-	-	-	-	-	-	-	CLOCK1	BOOT_MODE1
GPIO2	-	-	-	-	-	-	-	CLOCK2	BOOT_MODE2
GPIO3	-	-	-	-	-	-	-	CLOCK3	BOOT_MODE3
GPIO4	-	-	-	-	-	-	-	CLOCK4	BOOT_MODE4
GPIO5	-	-	-	-	-	-	-	CLOCK5	-
GPIO6	-	-	-	-	-	-	-	CLOCK6	-
GPIO7	-	-	-	-	-	-	-	-	WAKEUP
GPIO8	-	-	XIO_SEL4	HOSTIF_CLE	-	-	-	-	-
GPIO9	-	-	-	-	-	-	AI2_OSCLK	-	-
GPIO10	-	VDO_D47	-	-	-	-	AO2_SD3/ AO2_WS	-	-
GPIO11	-	VDO_D46	-	-	-	-	AO2_SD2/ AO2_BCK	-	-
GPIO12	-	VDO_D45	-	-	-	-	AO2_SD1/ AO2_OSCLK	-	-
GPIO13	-	VDO_D44	-	-	-	-	AO2_SD0	-	-
GPIO14	VDI_HOR	-	-	-	-	-	-	-	-
GPIO15	VDI_VER	-	-	-	-	-	-	-	-
GPIO16	-	-	XIO_SEL3	HOSTIF_INT_N	-	-	-	-	-
GPIO17	VDI_V0	-	-	HOSTIF_RESET_N	-	USB_LED0	-	-	-
GPIO18	-	-	-	-	PCI_REQ_N	-	-	-	-
GPIO19	-	-	XIO_D15	HOSTIF_D15	-	-	-	-	-
GPIO20	-	-	XIO_D14	HOSTIF_D14	-	-	-	-	-
GPIO21	-	-	XIO_D13	HOSTIF_D13	-	-	-	-	-
GPIO22	-	-	XIO_D12	HOSTIF_D12	-	-	-	-	-
GPIO23	-	-	XIO_D11	HOSTIF_D11	-	-	-	-	-
GPIO24	-	-	XIO_D10	HOSTIF_D10	-	-	-	-	-
GPIO25	-	-	XIO_D9	HOSTIF_D9	-	-	-	-	-
GPIO26	-	-	XIO_D8	HOSTIF_D8	-	-	-	-	-

Table 18. Multiplexed GPIO functionality[1] *…continued*

GPIO pin	Interfaces with mutually exclusive functionality								
	Video input	Video output	Extended I/O	Host	PCI	USB	Audio[2]	Clocks	Generic
GPIO27	VDI_D23	VDO_D43	-	HOSTIF_D7	-	-	AO2_WS	-	-
GPIO28	VDI_D22	VDO_D42	-	HOSTIF_D6	-	-	AO2_BCK	-	-
GPIO29	VDI_D21	VDO_D41	-	HOSTIF_D5	-	-	AI2_SD3	-	-
GPIO30	VDI_D20	VDO_D40	-	HOSTIF_D4	-	-	AI2_SD2	-	-
GPIO31	VDI_D19	VDO_D39	-	HOSTIF_D3	-	-	AI2_SD1	-	-
GPIO32	VDI_D18	VDO_D38	-	HOSTIF_D2	-	-	AI2_SD0	-	-
GPIO33	VDI_D17	VDO_D37	-	HOSTIF_D1	-	-	AI2_WS	-	-
GPIO34	VDI_D16	VDO_D36	-	HOSTIF_D0	-	-	AI2_BCK	-	-
GPIO35	-	-	-	HOSTIF_RD_OE_N	PCI_GNT_B_N	-	-	-	-
GPIO36	-	-	-	HOSTIF_RW_N	PCI_GNT_A_N	-	-	-	-
GPIO37	-	-	-	HOSTIF_CS_N	PCI_REQ_A_N	-	-	-	-
GPIO38	VDI_V2	-	-	-	-	-	-	-	-
GPIO39	VDI_V1	-	-	-	-	USB_LED1	-	-	-
GPIO40	-	-	-	-	-	-	AI1_SD3/ AI2_BCK	-	-
GPIO41	-	-	-	-	-	-	AI1_SD2/ AI2_WS	-	-
GPIO42	-	-	-	-	-	-	AI1_SD1/ AI2_SD0	-	-
GPIO43	-	-	-	-	-	-	AI1_SD0	-	-
GPIO44	-	-	-	-	-	-	AI1_WS	-	-
GPIO45	-	-	-	-	-	-	AI1_BCK	-	-
GPIO46	-	-	-	-	-	-	AI12_OSCLK	-	-
GPIO47	-	-	-	-	-	USB_VBUS_FLT	-	-	-
GPIO48	-	-	-	-	-	USB_VBUS_PWE	-	-	-
GPIO49	-	-	-	-	-	-	AO1_SD3	-	-
GPIO50	-	-	-	-	-	-	AO1_SD2	-	-
GPIO51	-	-	-	-	-	-	AO1_SD1	-	-
GPIO52	-	-	-	-	-	-	AO1_SD0	-	-
GPIO53	-	-	XIO_SEL2	-	-	-	-	-	-

Table 18. Multiplexed GPIO functionality[1] *…continued*

GPIO pin	Interfaces with mutually exclusive functionality								
	Video input	Video output	Extended I/O	Host	PCI	USB	Audio[2]	Clocks	Generic
GPIO54	-	-	XIO_SEL1	-	-	-	-	-	-
GPIO55	-	-	XIO_SEL0	-	-	-	-	-	-
GPIO56	-	-	XIO_ACK	-	-	-	-	-	-
GPIO57	-	-	XIO_AD26	-	-	-	-	-	-
GPIO58	-	-	XIO_AD25	-	-	-	-	-	-
GPIO59	-	-	-	-	PCI_REQ_B_N	-	-	-	-
GPIO60	-	-	-	-	PCI_GNT_N	-	-	-	-

[1] See running text of this section for the boot process. For default configuration of GPIO pins and functionality see Table 19.

[2] Additional flexible configuration is possible through dedicated register settings for the audio interface.

Table 19. Default configuration

Default configuration		Default configuration		Default configuration		Default configuration	
Pin	**Function**	**Pin**	**Function**	**Pin**	**Function**	**Pin**	**Function**
GPIO0	GPIO0	GPIO16	XIO_SEL3	GPIO32	VDI_D18	GPIO48	USB_VBUS_PWE
GPIO1	GPIO1	GPIO17	VDI_V0	GPIO33	VDI_D17	GPIO49	AO1_SD3
GPIO2	GPIO2	GPIO18	PCI_REQ_N	GPIO34	VDI_D16	GPIO50	AO1_SD2
GPIO3	GPIO3	GPIO19	XIO_D15	GPIO35	PCI_GNT_B_N	GPIO51	AO1_SD1
GPIO4	GPIO4	GPIO20	XIO_D14	GPIO36	PCI_GNT_A_N	GPIO52	AO1_SD0
GPIO5	GPIO5	GPIO21	XIO_D13	GPIO37	PCI_REQ_A_N	GPIO53	XIO_SEL2
GPIO6	GPIO6	GPIO22	XIO_D12	GPIO38	VDI_V2	GPIO54	XIO_SEL1
GPIO7	GPIO7	GPIO23	XIO_D11	GPIO39	VDI_V1	GPIO55	XIO_SEL0
GPIO8	XIO_SEL4	GPIO24	XIO_D10	GPIO40	AI1_SD3	GPIO56	XIO_ACK
GPIO9	AI2_OSCLK	GPIO25	XIO_D9	GPIO41	AI1_SD2	GPIO57	XIO_AD26
GPIO10	AO2_SD3	GPIO26	XIO_D8	GPIO42	AI1_SD1	GPIO58	XIO_AD25
GPIO11	AO2_SD2	GPIO27	VDI_D23	GPIO43	AI1_SD0	GPIO59	PCI_REQ_B_N
GPIO12	AO2_SD1	GPIO28	VDI_D22	GPIO44	AI1_WS	GPIO60	PCI_GNT_N
GPIO13	AO2_SD0	GPIO29	VDI_D21	GPIO45	AI1_BCK	-	-
GPIO14	VDI_HOR	GPIO30	VDI_D20	GPIO46	AI1_OSCLK	-	-
GPIO15	VDI_VER	GPIO31	VDI_D19	GPIO47	USB_VBUS_FLT	-	-

8.2 Digital video input formats

The PNX1005 accepts several digital video input formats (see Table 20). For restrictions see Table 21.

Table 20. Digital video input formats[1]

Input pin	Digital input formats (mutually exclusive options)				
	2 × 8-bit		**8-bit and 8-bit**	**24-bit**	**15-bit**
	Dual *ITU656* embedded sync	**Dual *ITU656* external sync**	***ITU656* embedded sync and TS**	**RGB**	**Raw capture mode (DAB)**
VDI_CLK0	-	-	-	-	-
VDI_CLK1	ITU_CLK0	ITU_CLK0	ITU_CLK	-	D_CLK
VDI_CLK2	ITU_CLK1	ITU_CLK1	TS_CLK	-	-
VDI_V0	-	ITU_HOR1	-	-	D0
VDI_V1	-	ITU_VER1	-	-	D1
VDI_V2	-	-	TS_VALID	CLK_IN	D2
VDI_HOR	-	ITU_HOR0	TS_START	HSYNC_IN	D3
VDI_VER	-	ITU_VER0	TS_STOP	VSYNC_IN	D4
VDI_D0	ITU1_D0	ITU1_D0	TS_D0	R0	D5
VDI_D1	ITU1_D1	ITU1_D1	TS_D1	B0	D6
VDI_D2	ITU1_D2	ITU1_D2	TS_D2	G0	D7
VDI_D3	ITU1_D3	ITU1_D3	TS_D3	R1	D8
VDI_D4	ITU1_D4	ITU1_D4	TS_D4	B1	D9
VDI_D5	ITU1_D5	ITU1_D5	TS_D5	G1	D10

Table 20. Digital video input formats[1] ...continued

Input pin	Digital input formats (mutually exclusive options)				
	2 × 8-bit		8-bit and 8-bit	24-bit	15-bit
	Dual *ITU656* embedded sync	Dual *ITU656* external sync	*ITU656* embedded sync and TS	RGB	Raw capture mode (DAB)
VDI_D6	ITU1_D6	ITU1_D6	TS_D6	R2	D11
VDI_D7	ITU1_D7	ITU1_D7	TS_D7	B2	D12
VDI_D8	ITU2_D0	ITU2_D0	ITU_D0	G2	-
VDI_D9	ITU2_D1	ITU2_D1	ITU_D1	R3	-
VDI_D10	ITU2_D2	ITU2_D2	ITU_D2	B3	-
VDI_D11	ITU2_D3	ITU2_D3	ITU_D3	G3	-
VDI_D12	ITU2_D4	ITU2_D4	ITU_D4	R4	-
VDI_D13	ITU2_D5	ITU2_D5	ITU_D5	B4	-
VDI_D14	ITU2_D6	ITU2_D6	ITU_D6	G4	-
VDI_D15	ITU2_D7	ITU2_D7	ITU_D7	R5	-
VDI_D16	-	-	-	B5	D13
VDI_D17	-	-	-	G5	D14
VDI_D18	-	-	-	R6	-
VDI_D19	-	-	-	B6	-
VDI_D20	-	-	-	G6	-
VDI_D21	-	-	-	R7	-
VDI_D22	-	-	-	B7	-
VDI_D23	-	-	-	G7	-

[1] For pinning see Table 6 and Table 18. For restrictions see Table 21.

Table 21. Restrictions on digital video input formats

Restriction on	Digital input formats (mutually exclusive options)				
	2 × 8-bit		8-bit and 8-bit	24-bit	15-bit
	Dual *ITU656* embedded sync	Dual *ITU656* external sync	*ITU656* embedded sync and TS	RGB	Raw capture mode (DAB)
Maximum number of audio I/Os	4	4	4	4	-
Host interface	-	-	-	cannot be used	-
Video output	-	-	-	restricted to 2 × 18-bit	-

9. Limiting values

Table 22. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Analog supplies						
$V_{DDA(CAB)(1V2)}$	CAB analog supply voltage (1.2 V)			–0.5	+1.5	V
$V_{DDA(CAB)(3V3)}$	CAB analog supply voltage (3.3 V)			–0.5	+3.8	V
$V_{DDA(CAB/DDS)}$	CAB/DDS analog supply voltage			–0.5	+1.5	V
$V_{DDA(CGU/PLL)}$	CGU/PLL analog supply voltage			–0.5	+1.5	V
$V_{DDA(DDR/PLL)}$	DDR/PLL analog supply voltage			–0.5	+1.5	V
$V_{DDA(DLL0)}$	DLL0 analog supply voltage			–0.5	+1.5	V
$V_{DDA(DLL1)}$	DLL1 analog supply voltage			–0.5	+1.5	V
$V_{DDA(DLL2)}$	DLL2 analog supply voltage			–0.5	+1.5	V
$V_{DDA(OSC)}$	oscillator analog supply voltage			–0.5	+1.5	V
$V_{DDA(DRV)(USB)}$	USB driver analog supply voltage			–0.5	+4.0	V
$V_{DDA(FB)(1V2)}$	Fuse Box analog supply voltage (1.2 V)			–0.5	+1.5	V
$V_{DDA(USB)}$	USB analog supply voltage			–0.5	+4.0	V
Digital supplies						
$V_{DDD(C)}$	core digital supply voltage			–0.5	+1.5	V
$V_{DDD(IO)}$	I/O digital supply voltage			–0.5	+3.8	V
$V_{DDD(IO)(DDR)}$	DDR I/O digital supply voltage			–0.5	+3.0	V
$V_{DDD(IO)(PCI)}$	PCI I/O digital supply voltage			–0.5	+5.5	V
Temperature						
T_{stg}	storage temperature			–40	+150	°C
T_{amb}	ambient temperature			0	70	°C
Input voltages						
V_I	input voltage	5 V tolerant inputs		–0.5	5.5	V
		3.3 V tolerant inputs; with $V_{DDD(IO)}$		–0.5	3.8	V
		1.8 V and 2.5 V tolerant inputs; with $V_{DDD(IO)(DDR)}$		–0.5	3.0	V
V_{esd}	electrostatic discharge voltage	human body model	[1]	-	±2000	V
		machine model	[2]	-	±200	V
		charge device model	[3]			
		corner pins		-	±750	V
		all other pins		-	±500	V

[1] Class 2 according to *JEDEC JESD22-A114*.

[2] Class B according to *JEDEC JESD22-A115*.

[3] Class III following *JEDEC JESD22-C101*.

10. Thermal characteristics

Table 23. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1][2]	20	K/W

[1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly. An ample amount of copper area directly under the PNX1005 with a number of through-hole plating, which connect to the ground layer (four-layer board: second layer), can also reduce the effective $R_{th(j-a)}$. Do not use any solder-stop varnish under the chip. In addition the use of soldering glue with a high thermal conductance after curing is recommended.

[2] The customer PCB must be reviewed by NXP experts to check the thermal resistance of the system.

11. Static characteristics

Operating conditions for minimum and maximum values in Table 25 to Table 31 hold for conditions given in Table 24 and T_{amb} = 0 °C to T_{amb} =70 °C, unless otherwise stated.

Table 24. Characteristics (supply pins)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog supplies						
$V_{DDA(CAB)(1V2)}$	CAB analog supply voltage (1.2 V)		1.16	1.20	1.24	V
$V_{DDA(CAB)(3V3)}$	CAB analog supply voltage (3.3 V)		3.15	3.30	3.45	V
$V_{DDA(CAB/DDS)}$	CAB/DDS analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(CGU/PLL)}$	CGU/PLL analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(DDR/PLL)}$	DDR/PLL analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(DLL0)}$	DLL0 analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(DLL1)}$	DLL1 analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(DLL2)}$	DLL2 analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(OSC)}$	oscillator analog supply voltage		1.16	1.20	1.24	V
$V_{DDA(DRV)(USB)}$	USB driver analog supply voltage		3.15	3.30	3.45	V
$V_{DDA(FB)(1V2)}$	Fuse Box analog supply voltage (1.2 V)		1.16	1.20	1.24	V
$V_{DDA(USB)}$	USB analog supply voltage		3.15	3.30	3.60	V
Digital supplies						
$V_{DDD(C)}$	core digital supply voltage		1.16	1.20	1.24	V
$V_{DDD(IO)}$	I/O digital supply voltage		3.15	3.30	3.45	V
$V_{DDD(IO)(DDR)}$	DDR I/O digital supply voltage	normal mode (DDR2)	1.70	1.80	1.90	V
		333 MHz to 400 MHz (DDR1)	2.40	2.55	2.70	V
$V_{DDD(IO)(PCI)}$	PCI I/O digital supply voltage	with 3.3 V supply	3.00	3.30	3.60	V
		with 5 V supply	4.75	5.00	5.25	V

Table 24. Characteristics (supply pins) *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power dissipation						
P_{tot}	total power dissipation	for all supplies	-	2.07	-	W
		for $V_{DDD(C)}$	-	1.20	-	W
		for $V_{DDD(IO)(DDR)}$	-	0.54	-	W
		for $V_{DDD(IO)}$	-	0.33	-	W

[1] <Table notes: delete section if not required>

Table 25. Characteristics (type P pins[1][2])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	5 V	$0.7 \times V_{DDD}$	-	5.3	V
		3.3 V	$0.7 \times V_{DDD}$		$V_{DDD} + 0.3$	
V_{IL}	LOW-level input voltage	5 V or 3.3 V	–0.3	-	$+0.3 \times V_{DDD}$	V
V_{OH}	HIGH-level output voltage		$0.9 \times V_{DDD}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.1 \times V_{DDD}$	V
t_f	fall time	between $0.2 \times V_{DDD}$ and $0.6 \times V_{DDD}$	1.3	-	-	ns
C_i	input capacitance		-	-	8	pF

[1] See Table 17.

[2] In this context V_{DDD} means $V_{DDD(IO)(PCI)}$.

Table 26. Characteristics (type I2 pins[1])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.3	-	5.3	V
V_{IL}	LOW-level input voltage		–0.3	-	+1.0	V
V_{OL}	LOW-level output voltage		-	-	0.6	V
V_{hys}	hysteresis voltage		0.25	-	-	V
t_f	fall time	C_L = 10 pF to 400 pF	1.5	-	250	ns
C_i	input capacitance		-	-	6	pF

[1] See Table 17.

Table 27. Characteristics (type H pins[1])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DDD(IO)}$	-	$V_{DDD(IO)} + 0.3$	V
V_{IL}	LOW-level input voltage		–0.3	-	$+0.3 \times V_{DDD(IO)}$	V
V_{OH}	HIGH-level output voltage		$0.9 \times V_{DDD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.1 \times V_{DDD(IO)}$	V
I_{OH}	HIGH-level output current	at $V_{OH} = V_{DDD(IO)}$ - 0.4 V	16	-	-	mA
I_{OL}	LOW-level output current	at V_{OL} = 0.4 V	16	-	-	mA
I_{pu}	pull-up current		25	50	85	µA
I_{pd}	pull-down current		25	50	85	µA

Table 27. Characteristics (type H pins[1]) *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time		0.5	-	1.0	ns
t_f	fall time		0.5	-	1.5	ns
C_i	input capacitance		-	-	3	pF
Z_o	output impedance		15	20	25	Ω

[1] See Table 17.

Table 28. Characteristics (type L pins[1])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DDD(IO)}$	-	$V_{DDD(IO)} + 0.3$	V
V_{IL}	LOW-level input voltage		–0.3	-	$+0.3 \times V_{DDD(IO)}$	V
V_{OH}	HIGH-level output voltage		$0.9 \times V_{DDD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.1 \times V_{DDD(IO)}$	V
V_{hys}	hysteresis voltage		$0.1 \times V_{DDD(IO)}$	-	-	V
I_{OH}	HIGH-level output current	at $V_{OH} = V_{DDD(IO)} - 0.4$ V	4.0	-	-	mA
I_{OL}	LOW-level output current	at $V_{OL} = 0.4$ V	4.0	-	-	mA
I_{pu}	pull-up current		25	50	85	µA
I_{pd}	pull-down current		25	50	85	µA
t_r	rise time		0.5	-	1.5	ns
t_f	fall time		0.5	-	1.8	ns
C_i	input capacitance		-	-	3.5	pF
Z_o	output impedance		40	50	60	Ω

[1] See Table 17.

Table 29. Characteristics (type F pins[1])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DDD(IO)}$	-	$V_{DDD(IO)} + 0.3$	V
V_{IL}	LOW-level input voltage		–0.3	-	$+0.3 \times V_{DDD(IO)}$	V
V_{OH}	HIGH-level output voltage		$0.9 \times V_{DDD(IO)}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.1 \times V_{DDD(IO)}$	V
V_{hys}	hysteresis voltage		$0.1 \times V_{DDD(IO)}$	-	-	V
I_{pu}	pull-up current		25	50	85	µA
I_{pd}	pull-down current		25	50	85	µA
t_r	rise time		1	-	2	ns
t_f	fall time		1	-	2	ns
C_i	input capacitance		-	-	4	pF
Z_o	output impedance		40	50	60	Ω

[1] See Table 17.

Table 30. Characteristics (type S pins[1][2])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DDD}$	-	$V_{DDD} + 0.3$	V
V_{IL}	LOW-level input voltage		–0.3	-	$+0.3 \times V_{DDD}$	V
V_{OH}	HIGH-level output voltage		$0.9 \times V_{DDD}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.1 \times V_{DDD}$	V
V_{hys}	hysteresis voltage		$0.1 \times V_{DDD}$	-	-	V
I_{pu}	pull-up current		25	50	85	µA
I_{pd}	pull-down current		25	50	85	µA
t_r	rise time		2	-	4	ns
t_f	fall time		2	-	4	ns
C_i	input capacitance		-	-	4.5	pF
Z_o	output impedance		40	50	60	Ω

[1] See Table 17.

[2] In this context V_{DDD} means $V_{DDD(IO)(DDR)}$.

Table 31. Characteristics (type T pins[1][2])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		$0.7 \times V_{DDD}$	-	$V_{DDD} + 0.3$	V
V_{IL}	LOW-level input voltage		–0.3	-	$+0.3 \times V_{DDD}$	V
V_{OH}	HIGH-level output voltage		$0.9 \times V_{DDD}$	-	-	V
V_{OL}	LOW-level output voltage		-	-	$0.1 \times V_{DDD}$	V
V_{hys}	hysteresis voltage		$0.1 \times V_{DDD}$	-	-	V
I_{pu}	pull-up current		25	50	85	µA
I_{pd}	pull-down current		25	50	85	µA
t_r	rise time		2	-	4	ns
t_f	fall time		2	-	4	ns
C_i	input capacitance		-	-	4.5	pF
Z_o	output impedance		40	50	60	Ω

[1] See Table 17.

[2] In this context V_{DDD} means $V_{DDD(IO)(PCI)}$.

Table 32. Characteristics (type U pins[1])

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog input (pin USB_VBUS)						
$V_{A\_SESS\_VLD}$	A-device session valid voltage		0.8	-	2	V
$V_{A\_VBUS\_VLD}$	A-device V_{BUS} valid voltage		4.4	-	-	V
$V_{B\_SESS\_VLD}$	B-device session valid voltage		2	-	4	V
$V_{B\_SESS\_END}$	B-device session end voltage		0.2	-	0.8	V
Analog inputs and outputs (pins USB_DM and USB_DP)						
V_{CM}	differential common mode voltage range		800	-	2500	mV
V_{DI}	differential input sensitivity voltage		100	400	1100	mV
V_{HSCM}	high-speed data signaling common mode voltage range (guideline for receiver)		–50	+200	+500	mV

[1] See Table 17.

12. Dynamic characteristics

Operating conditions for minimum and maximum values in Table 33 to Table 39 hold for conditions given in Table 24 and T_{amb} = +25°C, unless otherwise stated.

Table 33. Characteristics (DDR SDRAM memory interface)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock (pins MM_CLK_N and MM_CLK_P)						
f_{clk}	clock frequency	DDR2 mode	125	-	266	MHz
		DDR1 mode	83	-	200	MHz
t_{sk}	skew time	between MM_CLK_N and MM_CLK_P	–10	0	+10	ps
t_{PD}	propagation delay	on PCB	–240	0	+240	ps
Control and data						
t_{PD}	propagation delay	on PCB				
		pins MM_A[13:0], MM_CAS_N, MM_CKE, MM_CS_N, MM_RAS_N and MM_WE_N	–480	0	+480	ps
		pins MM_DS_N[3:0] and MM_DS_P[3:0]	–120	0	+120	ps
		pins MM_D[31:0] and MM_DM[3:0]	0	-	240	ps

Table 34. Characteristics (VDI interface)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock						
f_{clk}	clock frequency	pins VDI_CLK2 to VDI_CLK0	-	-	157	MHz
		pin VDI_D2, when used as *dv0_clkn*	-	-	108	MHz
		pin VDI_D3, when used as *dv1_clkn*	-	-	108	MHz
Control and data (pins VDI_CLK2 to VDI_CLK0, VDI_D[23:0], VDI_HOR and VDI_VER)						
$t_{su(i)}$	input set-up time	[1]	2	-	-	ns
$t_{h(i)}$	input hold time	[1]	2	-	-	ns
Additional timing						
$T_{VDI-ISU}$	VDI_D[23:0], VDI_HOR and VDI_VER to VDI{0,1,2}_CLK and VDI_D[3:2] (when applicable) input setup time	[2]	2	-	-	ns
T_{VDI-IH}	VDI_D[23:0], VDI_HOR and VDI_VER to VDI{0,1,2}_CLK and VDI_D[3:2] (when applicable) input hold time	[2]	2	-	-	ns

[1] The reference clock depends on the operating mode.

[2] See Figure 9.

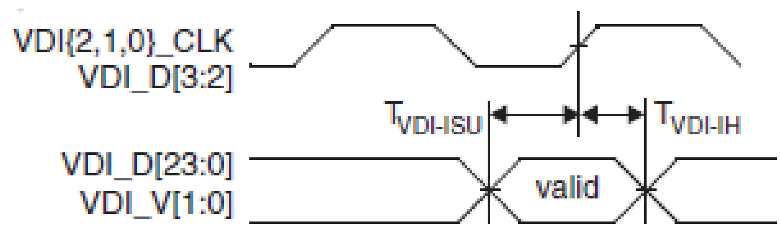


Fig 9. VDI interface timing

Table 35. Characteristics (VDO interface)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock (pin VDO_CLK)							
f_{clk}	clock frequency	VDO_MODE.QVCP_MODE = logic 1 and VDO_MODE.QVCP_DUAL_EDGE = logic 0	[1][2][3]	-	-	157	MHz
		VDO_MODE.QVCP_MODE = logic 1 and VDO_MODE.QVCP_DUAL_EDGE = logic 1	[1][3]	-	-	81	MHz
		VDO_MODE.VDO_BUFFER_MODE = logic 1	[1][3]	-	-	30	MHz
Data, see Figure 10							
$t_{d(DV)}$	data input valid delay time	QVCP block: VDO_CLK referenced to pins VDO[29:0], VDO_AUX1, VDO_HORand VDO_VER; VDO_MODE.QVCP_MODE = logic 1 ; VDO_CLK as input	[1]	3	-	9	ns
		Buffer: VDO_CLK referenced to pins VDO[47:0], VDO_AUX1, VDO_HOR and VDO_VER; VDO_MODE.VDO_BUFFER_MODE = logic 1	[1][3]	5	-	20	ns
$t_{d(QV)}$	data output valid delay time	QVCP block: VDO_CLK referenced to pins VDO[29:0], VDO_AUX1, VDO_HOR and VDO_VER; VDO_MODE.QVCP_MODE = logic 1 ; VDO_CLK as output	[1]	1.2	-	3.9	ns
$t_{su(i)}$	input set-up time	VDO_VER to VDO_CLK	[1][3]	3	-	-	ns
$t_{h(i)}$	input hold time	VDO_VER to VDO_CLK	[1][3]	2	-	-	ns

[1] VDO_MODE.QVCP_MODE and VDO_MODE.VDO_BUFFER_MODE are mutually exclusive.

[2] When pin VDO_CLK is set as an input, the AC timing of the remaining VDO pins may not allow to run at the maximum operating frequency.

[3] Data are the same for both input or output mode of pin VDO_CLK.

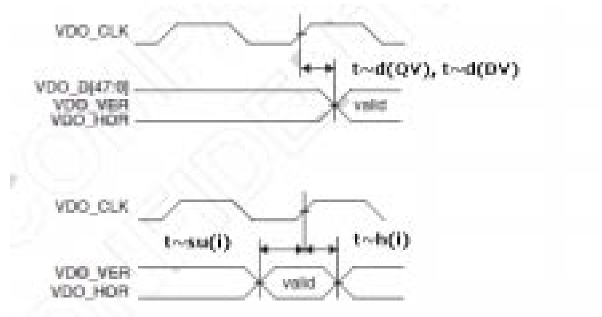


Fig 10. VDO interface timing

Table 36. Characteristics (digital audio input interface)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
f_{clk}	clock frequency	AI12_OSCLK and AI2_OSCLK		-	-	50	MHz
		AI1_BCK and AI2_BCK		-	-	27	MHz
Data, see Figure 11							
t_{PD}	propagation delay	AI1_BCK to AI1_WS; AI2_BCK to AI2_WS	[1]	4	-	12	ns
$t_{su(i)}$	input set-up time	AI1_SD[3:0], AI1_WS to AI1_BCK; AI2_SD[3:0], AI_WS2 to AI2_BCK	[1]	4	-	-	ns
$t_{h(i)}$	input hold time	AI1_SD[3:0], AI1_WS to AI1_BCK; AI2_SD[3:0], AI_WS2 to AI2_BCK	[1]	0	-	-	ns

[1] Data are the same for both input or output mode of pins AI1_BCK or AI2_BCK (master or slave). They hold for both rising or falling edge. For functional pins see Section 8.1.

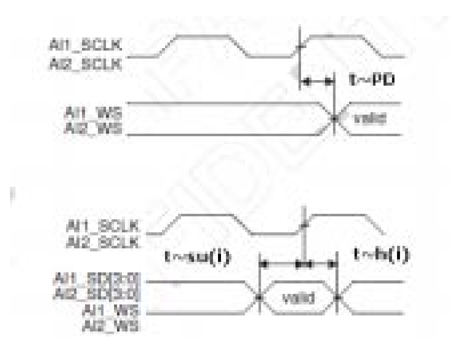


Fig 11. AI interface timing

Table 37. Characteristics (digital audio output interface)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
f_{clk}	clock frequency	AO12_OSCLK and AO2_OSCLK		-	-	50	MHz
		AO12_BCK and AO2_BCK		-	-	27	MHz
Data, see Figure 12							
t_{PD}	propagation delay	AO12_BCK to AO1_SD[3:0], AO2_SD[3:0], AO12_WS; AO2_BCK to AO2_SD[3:0], AO2_WS	[1]	4	-	12	ns
$t_{su(i)}$	input set-up time	AO12_WS to AO12_BCK; AO2_WS to AO2_BCK	[1]	4	-	-	ns
$t_{h(i)}$	input hold time	AO12_WS to AO12_BCK; AO2_WS to AO2_BCK	[1]	0	-	-	ns

[1] Data are the same for both input or output mode of pins AI1_BCK or AI2_BCK (master or slave). They hold for both rising or falling edge. For functional pins see Section 8.1.

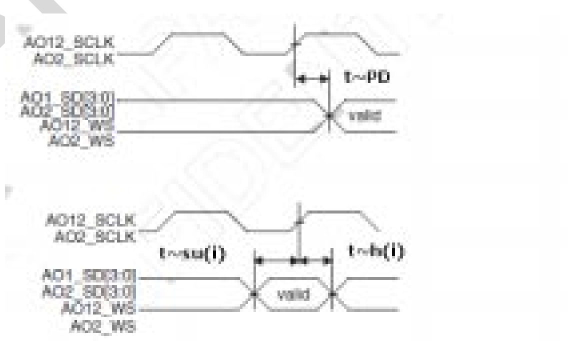


Fig 12. AO interface timing

Table 38. Characteristics (GPIO interface)[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock							
f_{clk}	clock frequency		[2]	-	-	108	MHz
Data, see Figure 13							
t_{PD}	propagation delay	CLOCK[6:0] to GPIO[7:0]	[3]	2	-	10	ns
		CLOCK[6:0] to GPIO[60:8]]	[3]	4		12	ns

Table 38. Characteristics (GPIO interface)[1] *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{su(i)}$	input set-up time	GPIO[7:0] to CLOCK[6:0]	[3]	2	-	-	ns
		GPIO[60:8] to CLOCK[6:0]	[3]	5		-	ns
$t_{h(i)}$	input hold time	GPIO[7:0] to CLOCK[6:0]	[3]	2	-	-	ns
		GPIO[60:8] to CLOCK[6:0]	[3]	4	-	-	ns

[1] See Table 18.

[2] The maximum operating frequency may be lower due to the wide variation of t_{PD}.

[3] Data are the same for both input or output mode of these pins. They hold for both rising or falling edge.. See table note in Table 9 for clock and data assignments.

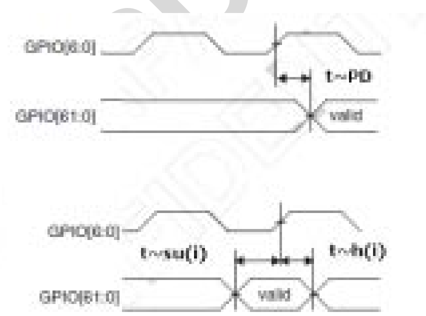


Fig 13. GPIO interface timing

Table 39. Characteristics (PCI-bus and XIO interface)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clock (pins PCI_CLK and PCI_SYS_CLK)							
T_{cy}	cycle time			15	-	-	ns
t_{high}	CLK high time			6	-	-	ns
t_{low}	CLK low time			6	-	-	ns
t_{val}	CLK to signal valid delay time - bused signal		[1]	2	-	6	ns
$t_{val(ptp)}$	CLK to signal valid delay time - point-to-point		[1]	2	-	6	ns
t_{on}	float to active delay time			2	-	-	ns
t_{off}	active to float delay time			-	-	14	ns
Data							
t_{su}	input set-up time to CLK - bused signal			3	-	-	ns
$t_{su(ptp)}$	input set-up time to CLK - point-to-point			5	-	-	ns
t_h	input hold time from CLK			0	-	-	ns
$t_{rst\text{-}off}$	reset active to output float delay time	pins RESET_IN_N and POR_IN_N		-	-	40	ns

Table 39. Characteristics (PCI-bus and XIO interface) *...continued*

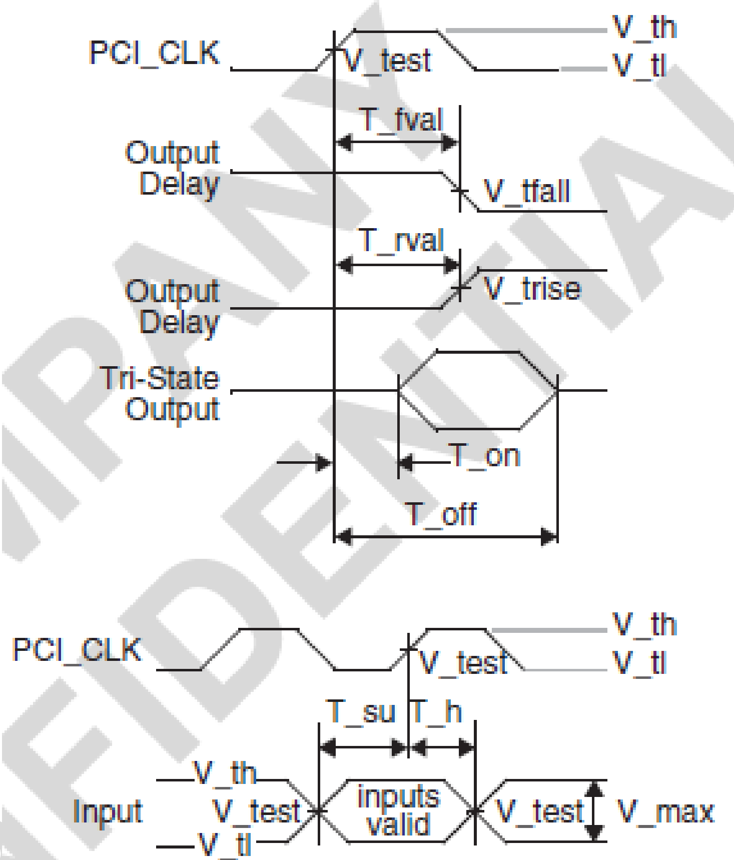
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{su}	input set-up time to CLK - bused signal						ns
t_h	input hold time from CLK	signals XIO_ACK and XIO_D[15:8]		0	-	-	ns
Additional timing; see Figure 14							
T_{PCI_CLK}	PCI_CLK and PCI_SYS_CLK cycle time		[2]	15	-	-	ns
$T_{PCI\_CLK\text{-}HL}$	PCI_CLK and PCI_SYS_CLK low and high time			6	-	-	ns
$T_{VAL\text{-}PCI}$	PCI_CLK to signal valid delay, bus signals		[3]	2	-	6	ns
$T_{VAL\text{-}PTP\text{-}PCI}$	PCI_CLK to signal valid delay, point-to-point signals		[3]	2	-	6	ns
$T_{ON\text{-}PCI}$	PCI float to active delay			2	-	-	ns
$T_{OFF\text{-}PCI}$	PCI active to float delay			-	-	14	ns
$T_{SU\text{-}PCI}$	PCI input setup time to PCI_CLK, bussed signals			3	-	-	ns
$T_{SU\text{-}PTP\text{-}PCI}$	PCI input setup time to PCI_CLK, point-to-point signals			5	-	-	ns
$T_{H\text{-}PCI}$	PCI input hold time from PCI_CLK			0	-	-	ns
$T_{RST\text{-}OFF\text{-}PCI}$	PCI reset (RESET_IN_N or POR_IN_N) active to output float delay			-	-	40	ns
$T_{VAL\text{-}XIO}$	PCI_CLK to XIO signals delay	pins XIO_AD[26:25], XIO_SEL[4:0] and XIO_D[15:8]	[4]	2	-	10	ns
$T_{SU\text{-}XIO}$	XIO input setup time to PCI_CLK	pins XIO_ACK and XIO_D[15:8]	[4]	9	-	-	ns
$T_{H\text{-}XIO}$	XIO input hold time from PCI_CLK	pins XIO_ACK and XIO_D[15:8]	[4]	0	-	-	ns

[1] Valid for all XIO signals from Table 18, besides XIO_ACK.

[2] PCI-bus and XIO interface

[3] See Figure 15 for ,easurement conditions of minimum and maximum values.

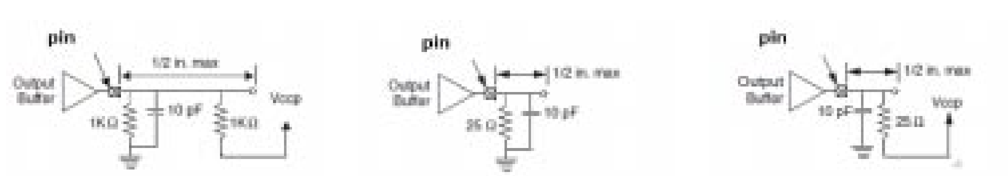
[4] See Table 18.



(1) 5 V signalling: V_{th} = 2.4 V, V_{tl} = 0.4 V and V_{max} = 2.0 V

(2) 3.3 V signalling: $V_{th} = 0.6 \times V_{DDD(IO)(PCI)}$, $V_{tl} = 0.2 \times V_{DDD(IO)(PCI)}$ and $V_{max} = 0.4 \times V_{DDD(IO)(PCI)}$

Fig 14. PCI-bus and XIO interface timing



a. Slew rate

b. Rising edge

c. Falling edge

Fig 15. Type P cell test load conditions; see Table 17

Table 40. Characteristics (host interface)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{HST\text{-}ACCESS}$	Access time, i.e. delay between two consecutive HOSTIF_CS_N falling edges.		[1]	40	-	-	ns
$T_{HST\text{-}WR\text{-}ISU}$	HOSTIF_D[15:0] and HOSTIF_CLE rising edge to rising edge of HOSTIF_RW_N and rising edge of HOSTIF_CS_N input setup time	see Figure 16	[1]	10	-	-	ns
$T_{HST\text{-}WR\text{-}IH}$	HOSTIF_D[15:0] and falling edge of HOSTIF_CLE to rising edge of HOSTIF_RW_N or rising edge of HOSTIF_CS_N input hold time		[1]	5	-	-	ns
$T_{HST\text{-}WR\text{-}DLY}$	Delay between a rising edge on HOSTIF_RW_N and a falling edge on HOSTIF_CS_N, i.e. delay between end of write and next access.		[1]	10	-	-	ns
$T_{HST\text{-}RD\text{-}DV}$	Falling edge of HOSTIF_RD_OE_N and falling edge of HOSTIF_CS_N to HOSTIF_D[15:0] output delay		[2]	2.5	-	13	ns
$T_{HST\text{-}RD\text{-}OH}$	Rising edge of HOSTIF_RD_OE_N and rising edge of HOSTIF_CS_N to HOSTIF_D[15:0] output hold time		[2]	2.5	-	13	ns

[1] HOSTIF_RD_OE_N is constant logic 1 during a write command.

[2] HOSTIF_WR_N is a constant logic 1 and HOSTIF_CLE is a constant logic 0 during read command.

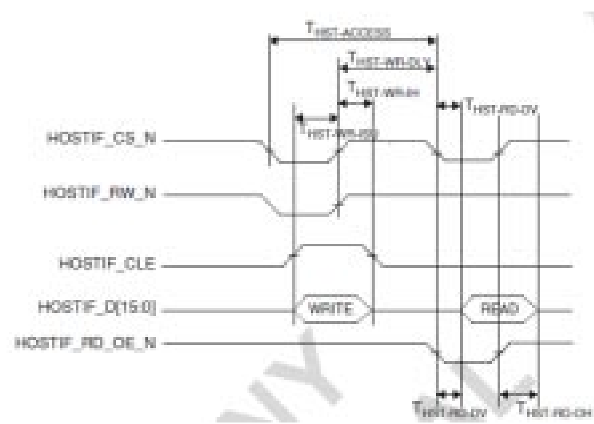


Fig 16. Host interface timing

Table 41. Characteristics (reset interface[1][2], see Figure 17)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{LOWPP}	POR_IN_N reset active time after power stable		1	-	-	ms
T_{LOWP}	POR_IN_N reset active time after power and clock stable		100	-	-	µs
T_{LOWR}	RESET_IN_N active time		100	-	-	µs

[1] POR_IN_N and RESET_IN_N are asynchronous signals.

[2] At power-up only POR_IN_N is required to be asserted. RESET_IN_N can be used as warm reset and left unconnected if not used as warm reset. Note that the JTAG state machines do not get reset when only RESET_IN_N is being asserted low.

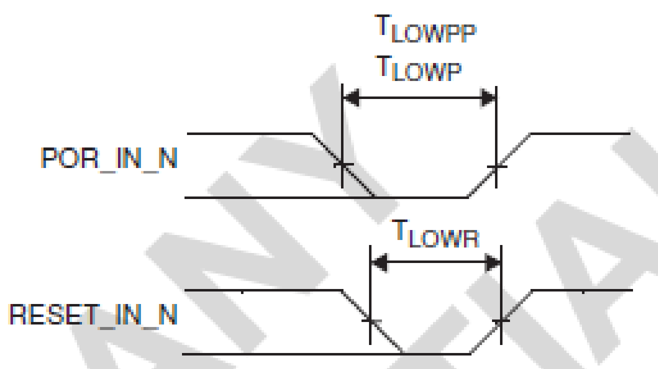


Fig 17. Reset interface timing

Table 42. Characteristics (I^2C-bus interface)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock						
f_{clk}	clock frequency		-	-	400	kHz
Data, see Figure 18						
$T_{SCL-BUF}$	Bus free time		1	-	-	µs
$T_{SCL-LOW}$	IIC_SCL low time		1	-	-	µs
$T_{SCL-HIGH}$	IIC_SCL high time		1	-	-	µs
T_{BUF}	IIC_SCL and IIC_SDA fall time (Cb = 10-400 pF, from V_{IH-IIC} to V_{IL-IIC})		20 + 0.1 × C_b	-	250	ns
T_{SU-STA}	Start condition set up time		1	-	-	µs
T_{H-STA}	Start condition hold time		1	-	-	µs
T_{SDA-SU}	Data setup time		100	-	-	ns
T_{SDA-H}	Data hold time		0	-	-	ns
T_{SDA-DV}	IIC_SCL LOW to data out valid		-	-	0.5	µs
T_{STO-DV}	IIC_SCL HIGH to data out		1	-	-	ns

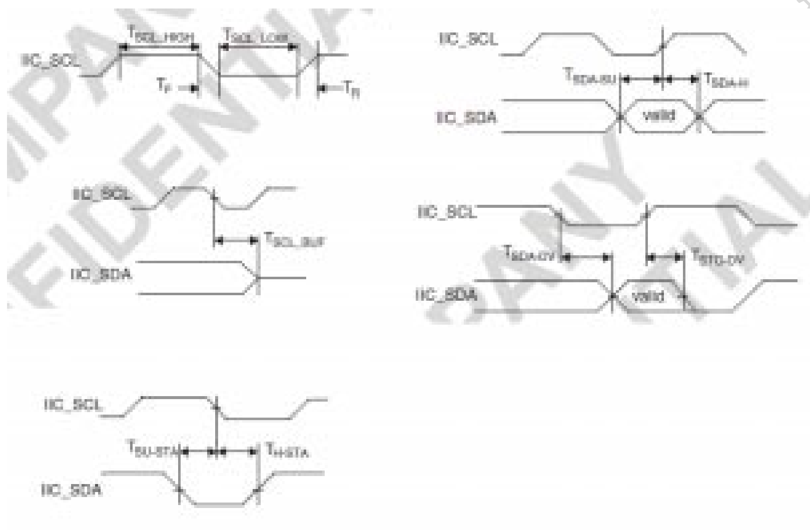


Fig 18. I²C-bus interface timing

Table 43. Characteristics (JTAG interface)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Clock						
f_{clk}	clock frequency	boundary scan	-	-	25	MHz
		operating frequency	-	-	50	MHz
Data, see Figure 19						
t_{PD}	propagation delay		0	-	5	ns
$t_{su(i)}$	input set-up time		5	-	-	ns
$t_{h(i)}$	input hold time		3	-	-	ns

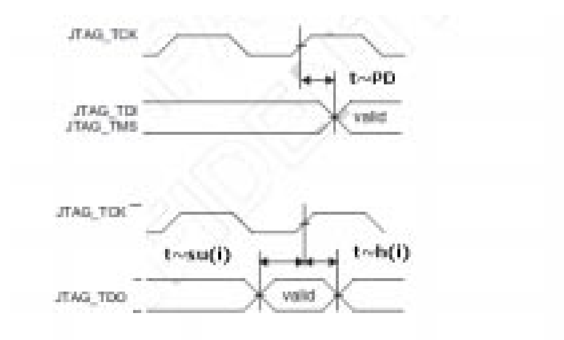


Fig 19. JTAG interface timing

13. External crystal

13.1 With external crystal HC-49U

Table 44. Characteristics (external crystal HC-49U, pin XTAL_I)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{xtal}	crystal frequency	fundamental mode	-	27.000 00	-	MHz
$\Delta f_{xtal(T)}/f_{xtal}$	relative crystal frequency variation with temperature		-	±30	-	ppm
T_{amb}	ambient temperature		–40	-	+85	°C
C_{ext}	external capacitance		-	-	18	pF
C_L	load capacitance		-	18	-	pF
C_{shunt}	shunt capacitance		-	-	7	pF
R_{ESR}	equivalanent series resistance		-	-	130	Ω
P_{drive}	drive power		-	-	1	mW

13.2 In oscillator mode

Table 45. Characteristics (in oscillator mode, pin XTAL_I)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta f_{xtal(T)}/f_{xtal}$	relative crystal frequency variation with temperature		-	±30	-	ppm
δ	duty cycle		45	-	55	%
T_{amb}	ambient temperature		–40	-	+85	°C
C_{shunt}	shunt capacitance		-	-	7	pF

14. Package outline

Fig 20. Package outline SOT1136-1 (BGA420)

Remark: Package SOT1136-1 currently is under qualification

Fig 21. Soldering footprint SOT1136-1 (BGA420)

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 22) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 46 and 47

Table 46. SnPb eutectic process (from J-STD-020C)

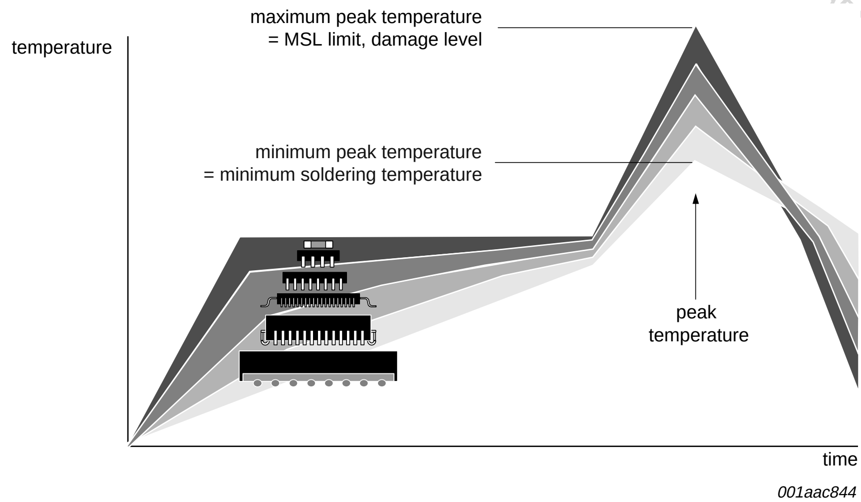
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 47. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 22.



MSL: Moisture Sensitivity Level

Fig 22. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

16. Abbreviations

Table 48. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AI	Audio Input
AI2	Audio Input 2 interface
AO	Audio Output
AO2	Audio Output 2 interface
BOM	Bill Of Materials
CAB	Custom Analog Block
CD	Compact Disc
CGU	Clock Generation Unit
CPU	Central Processing Unit
DAB	Digital Audio Broadcast
DAC	Digital-to-Analog Converter
DCS	Device Status and Control
DDR	Double Data Rate
DDS	Direct Digital Synthesis
DLL	Delay-Locked Loop
DLNA	Digital Living Network Alliance[1]
DMA	Direct Memory Access
DTL	Device Transaction Level
DV	Digital Video
DVD	Digital Versatile Disc
DVD-D	DVD-Descrambler
EDDI	Edge-Dependent De-Interlacing
EJTAG	Enhanced JTAG
FB	Fuse Box
FGPI	Fast General Purpose Interface
FIFO	First-In First-Out
FIR	Finite Impulse Response
FSE	Front Seat Entertainment
GPIO	General Purpose Input and Output
GUI	Graphical User Interface
HD	High-Definition
HDD	Hard Disc Drive
HDTV	High-Definition TV
HS	High-Speed
IC	Integrated Circuit
IDE	Integrated Drive Electronics
I^2C-bus	Inter-IC bus
I^2S	Inter-IC Sound

Table 48. Abbreviations *…continued*

Acronym	Description
I/O	Input/Output
ITU	International Telecommunication Union
JEDEC	Joint Electron Device Engineering Council[2]
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LSB	Least Significant Bit
LUT	Look-Up Table
MBS	Memory Based Scaler
MMIO	Memory Mapped I/O
MPEG	Moving Picture Expert Group
MSB	Most Significant Bit
NTSC	National Television Standards Committee
OSD	On-Screen Display
OTG	On-The-Go
PAL	Phase Alternating Line
PCI-bus	Peripheral Component Interconnect-bus
PI	Programming Interface
PIO	Programming I/O
PLL	Phase-Locked Loop
QVCP	Quality Video Composition Processor
RAM	Random Access Memory
RGB	Red Green Blue
RSE	Rear Seat Entertainment
R/W	Read/Write
SD card	Secure Digital card
SDRAM	Synchronous Dynamic RAM
SDTV	Standard-Definition TV
SW	SoftWare
TM	TriMedia
TS	Transport Stream
TSU	Time Stamp Unit
TV	TeleVision
UI	User Interface
USB	Universal Serial Bus
VBI	Vertical Blanking Interval
VDI	ViDeo Input
VDO	ViDeo Output
VDOB	ViDeo Out Buffer
VESA	Video Electronics Standards Association

Table 48. Abbreviations *…continued*

Acronym	Description
VGA	Video Graphics Array
VIP	Video Input Processor
XIO	eXtended I/O

[1] An international, cross-industry collaboration of consumer electronics, computing industry and mobile device companies.

[2] Nowadays called JEDEC Solid State Technology Association, or simply JEDEC.

17. Glossary

Bluetooth — A standard for wireless radio communications.

Co-sited video — The video pixel are more regularly distributed across the video memory.

DDR1 — Same as DDR, see Table 48.

DDR2 — DDR memory with 4-fold, instead of 2-fold, prefetch for high bandwidth storage.

FLASH memory — Non-volatile memory that can be electrically erased and programmed.

Interspersed video — The video pixel are interspersed in memory; the VDO module makes them accessible again.

UV — The U- and V-components of a YUV signal.

WiFi — Wireless technology used to connect portable devices to the car.

YUV — The color space used in the PAL analog television standard.

18. Revision history

Table 49. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PNX1005_1	<yyyymmdd>	Objective data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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